ATC2603C Datasheet

Version: 2.2

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Revision History

Date	Revision	Description
2014-08-30	1.0	First Release
2015-03-10	1.1	Correct some mistakes and add descriptions on ICMADC.
2015-06-03	1.2	Correct mistakes on LDO11 & LDO12 functions descriptions.
2015-06-25	2.0	Add electrical parameters tables and figures in Chap4
2015-07-30	2.1	1. Correct mistakes of pin68; 2. Update parameters and registers.
2015-09-23	2.2	Correct conflicts in LDO parameters

1 Introduction

1.1 Overview

ATC2603C is an integrated power management and audio subsystem which provides a cost effective, single-chip solution for portable multimedia systems. All the information from Master is configured through TWI (Two Wire Interface) interface of ATC2603C.

The integrated audio Codec provides all the necessary functions for high-quality recording and play-back. Programmable on-chip amplifiers allow direct connection of headphones and microphones with a minimum of external components.

ATC2603C includes three programmable DC-DC converters, eight low-dropout (LDO) regulators and one current limit switch to generate suitable supply voltage for the system, including on-chip audio CODEC as well as off-chip components such as a digital core and memory chips. Each of these is voltage programmable. ATC2603C can be powered by a lithium battery, wall adaptor or USB.

An on-chip battery charger supports both trickle charging and fast (Constant Current, Constant Voltage) charging of single-cell Lithium battery. The charging current, termination voltage, and time-out are programmable to fit different types of batteries.

Internal power management circuit controls the start-up and shutdown sequence of supply voltages, as well as sleep and wake-up. It also detects and handles abnormal conditions such as overvoltage, overcurrent, etc.

A 32.768 kHz crystal oscillator should be supplied to ATC2603C system to get an accuracy clock for real time clock (RTC) and get alarm function for waking up the system. The master clock can be input directly from Master. IR and multi-channel ADC capable of waking up the system are also integrated.

1.2 Features

Audio CODEC

- 2.0 channel DAC, SNR (A-WEIGHTING) > 98dB, THD < -80dB
- 2.0 channel ADC, SNR(A-WEIGHTING) > 91dB, THD < -82dB
- Stereo 20mW PA (Power Amplifier) for headphone with 41 level volume control(volume update with zero-cross detection), traditional mode and direct drive mode, both with anti-pop circuit
- DAC supports sample rate of 192k/176.4k/96k/48k/32k/24k/16k/12k/8k/88.2k/44.1k/22.05k/11.025k
- ADC supports sample rate of 96k/48k/32k/24k/16k/12k/8k/44.1k/22.5k/11.025k
- Configurable high-pass filter with ADC
- Slave mode I2S, TDM mode only, Tx and Rx both
- 2.0 channel I2S Receiver and 2.0 channel transmitter

- I2S supports sample rate of 192k/176.4k/96k/48k/32k/24k/16k/12k/8k/88.2k/44.1k/22.05k/ 11.025k

Power Supply Generation

3 DC-DCs

- DC-DC Buck Converter (0.7~1.4V, Up to 1200mA)
- DC-DC Buck Converter (1.3~2.2V, Up to 1000mA)
- DC-DC Buck Converter (2.6~3.3V, Up to 1000mA, when working without inductance, up to 800mA)

8LDOs and 1 SWITCH:

- LDO voltage regulators (2.6~3.3V, Up to 200mA), high PSRR(LDO1)
- LDO voltage regulators (2.6~3.3V, Up to 200mA), high PSRR(LDO2)
- LDO voltage regulator (1.5~2.0V, Up to 250mA) (LDO3)
- LDO voltage regulators (2.6~3.3V, Up to 150mA), high PSRR(LDO5)
- LDO voltage regulator (0.7~1.4V, Up to 200mA), high PSRR(LDO6)
- LDO voltage regulator (1.5~2.0V, Up to 200mA), high PSRR(LDO7)
- LDO voltage regulator (1.5~2.0V, Up to 5mA), for SVCC use(LDO11)
- LDO voltage regulator (2.6~3.3V, Up to 25mA), for RTCVDD use(LDO12)
- One SWITCH, configurable to LDO mode
- Overvoltage, Overcurrent, Overtemperature protection of DC-DCs and LDOs

Battery Charger

- Single-cell Lithium battery charger
- Thermal protection for charging control;

Power saving mode

- Several power saving modes including standby mode, sleep mode and deep-sleep mode
- “Always on” RTC with wake-up alarm
- In deep-sleep with RTC always on, the current of IBAT can be less than 30μA

System Control

- TWI slave Interface
- Handles power sequencing, power-on reset signal, sleep mode signal and interrupt signals
- Adaptive Power Distribute System, autonomous power source selection (Battery, Wall adaptor or USB bus)

Additional Features

- A multi-channel 10-bit ADC, can be used as voltage, current measurement or wake-up sources for Remote control
- An EXTIRQ to Master
- Configurable GPIO pins
- 24MHz system clock input supported
- ESD Level of HBM pass over 2000V of all IOs
- QFN68 package, 8mm*8mm, 0.4mm pin pitch

1.3 Typical Applications

ATC2603C mainly consists of Power Management Unit and Audio CODEC block targeted at multimedia platform application. Figure 1-1 below shows the typical application diagram of ATC2603C.

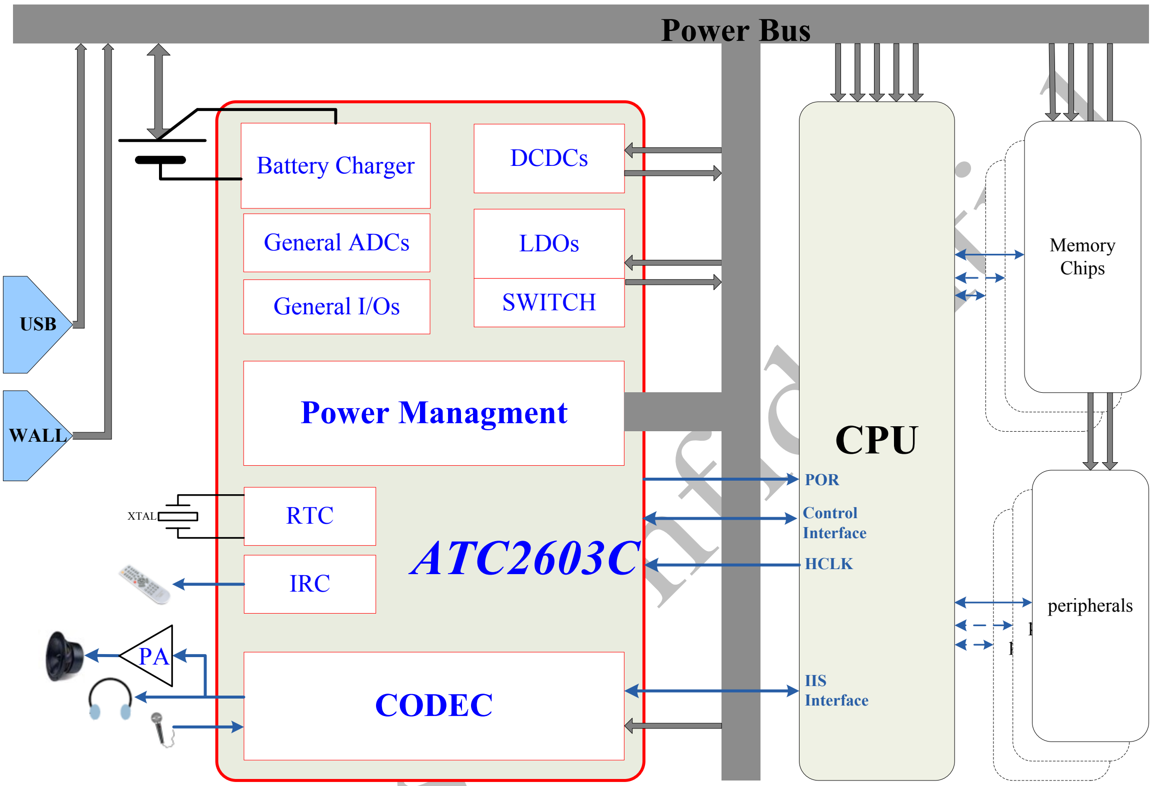


Figure 1-1 Typical Application diagram

1.4 Ordering Information

Table 1-1 Ordering Information

Part Numbers	Package	Size
ATC2603C	QFN68	8mm*8mm

2 Absolute Maximum Rating

These absolute maximum ratings are stress ratings, operating at or beyond these ratings for more than 1ms may result in permanent damage. Unless otherwise noted, all voltage values are relative to VSS.

Table 2-1 Max ratings of ATC2603C

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	TBD	TBD	℃
Storage Temperature	Tstg	-55	+150	℃
Supply Voltage	DCxIN/WALL/VBUS/BAT/SYSPWR	-0.5	+6.5	V
Input Voltage	Digital IO	-0.3	3.6	V
	Analog IO (FMIN/MICIN)	-0.3	3.6	V
ESD Stress Voltage	VESD (Human Body Model)	2000	-	V

3 Recommended Operating Conditions

Table 3-1 Recommended Operating Voltage

Parameter	Symbol	Min	Typ	Max	Unit
Wall adapter input source	WALL	4.3	-	5.5	V
USB VBUS input source	VBUS	4.75	-	5.25	V
Battery input source	BAT	3.0	-	4.2	V
Supply voltage	DCxVIN/LDOxIN/SWxIN	3.0	-	5.5	V
Core supply	VDD	-	1.8	-	V
IO supply	VCC	-	3.1	-	V
Ground	GND/AGND/DCxGND/CDPGNDx	-	0	-	V

Note: in DCxVIN/LDOxIN/SWxIN and DCxGND/CDPGNDx, x is number, for example, DC1VIN represents the Input Voltage of DC-DC1.

4 Electrical Characteristics

4.1 Overshoot

The maximum DC voltage on power supply pins is 6.5V. However, during voltage domains switching period, the device can tolerate overshoot for up to 10μs, as shown in Figure 4-1 below.

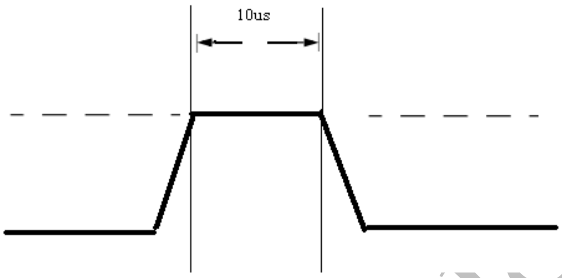


Figure 4-1 Tolerance for overshoot for up to 10μs

Table 4-1 Extreme Values for Input Pins

Parameter	Symbol	Start	Max	Unit
Supply voltage	DCxIN/WALL/VBUS/BAT	-0.3	12	V

ATC2603C can tolerate 1,000 times of such pulses. But exposed to overshoot circumstances for too many times may affect device's lifetime.

4.2 Powerpath

Table 4-2 Powerpath Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
V_{BUS}	Bus input voltage Range	4.5	5	5.5	V
V_{WALL}	Wall input voltage Range	4.5	5	5.5	V
V_{BAT}	Bat input voltage Range	3.3	4.2	4.4	V
$V_{out(BUS)}$	System Power Output Voltage		V_{BUS}-0.1	5	V
$V_{out(WALL)}$	System Power Output Voltage		V_{WALL}-0.1	5	V
$V_{out(BAT)}$	System Power Output Voltage		V_{BAT}-0.1	4.3	V
$R_{BUS(on)}$	Internal Ideal Resistance		450		mΩ
$R_{WALL(on)}$	Internal Ideal Resistance		300		mΩ
$R_{BAT(on)}$	Internal Ideal Resistance		300		mΩ
$V_{WK(BUS)}$	Wake Up Voltage	4.05	4.2	4.5	V
$V_{WK(WALL)}$	Wake Up Voltage	4.05	4.2	4.5	V
$V_{UV(BAT)}$	Under Voltage Int Threshold	3.1	3.3	3.5	V
$V_{OV(BAT)}$	Over Voltage Int Threshold	4.3	4.4	4.8	V
$I_{OC(BAT)}$	Over Current Protection Threshold	600	1000	1200	mA

$V_{UV(BUS)}$	Under Voltage Int Threshold	3.8	4.3	4.5	V
$V_{OV(BUS)}$	Over Voltage Int Threshold	5.5	6.3	6.8	V
$I_{OC(BUS)}$	Over Current Protection Threshold	600	1000	1200	mA
$V_{UV(WALL)}$	Under Voltage Int Threshold	3.8	4.5	4.5	V
$V_{OV(WALL)}$	Over Voltage Int Threshold	5.5	6.3	6.8	V
$I_{OC(WALL)}$	Over Current Protection Threshold	600	1000	1200	mA
$I_{LIMIT(BUS)}$	Bus Input Current Limited	300	500	1000	mA
$I_{LIMIT(WALL)}$	Wall Input Current Limited	300	500	2000	mA
$V_{LIMIT(BUS)}$	Bus Input Voltage Limited	4.2	4.3	4.5	V
$V_{LIMIT(WALL)}$	Wall Input Voltage Limited	4.2	4.3	4.5	V

4.3 DCDC

Table 4-3 DCDC1 Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
Vi	Input Voltage	3.2	-	5	V
Vo	Output Voltage	0.7	1.0	1.4	V
Io	Output Current Drivability △Vo/Vo=-5%		1200		mA
Fsw	Switching Frequency	0.85	1.6	2.7	MHz
Vripple	Output Ripple Voltage Vo=1.0V,Io=1000mA		10		mV
	Output Ripple Voltage Vo=1.0V,Io=20mA		60		
Eff	Efficiency Vi=3.8V Vo=1.0V,Io=400mA		85		%
Tpu	Power Up Time	15	20	30	us
Tpd	Power Down Time Io=10mA		5		ms
LNR	Line Regulation Vi=3.3V-5.0V,Io=1000mA		0.05		%/V
LDR	Load Regulation Vi=5V,Io=10mA-1000mA		0.05		%/A
LDTR	Load Transient Response Vi=5.0V,Io=10mA-1000mA,1us		30		mV
Iocp	Over Current Limit For Output		1800		mA
Vuvp	Under Voltage Int For Output		0.9*Vo		V
Vovp	Over Voltage Int For Output		1.1* Vo		V
R(P)	Power Mosfet Switches High-side		250		mΩ
L	External Inductance DCR<50mΩ		2.2		uH
C	External Capacitance ESR<50mΩ		10		uF

Table 4-4 DCDC2 Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
Vi	Input Voltage	3.2	4.1	5	V
Vo	Output Voltage	1.0	1.4	1.85	V
Io	Output Current Drivability ∆Vo/Vo=-5%		1000		mA
Fsw	Switching Frequency	0.85	1.6	2.7	MHz

Vripple	Output Ripple Voltage Vo=1.4V,Io=1000mA		10		mV
	Output Ripple Voltage Vo=1.4V,Io=20mA		70		
Eff	Efficiency Vi=3.8V Vo=1.4V,Io=300mA		89		%
Tpu	Power Up Time	20	30	60	us
Tpd	Power Down Time Io=10mA		5		ms
LNR	Line Regulation Vi=3.3V-5.0V,Io=1000mA		0.05		%/V
LDR	Load Regulation Vi=5.0V,Io=10mA-1000mA		0.05		%/A
LDTR	Load Transient Response Vi=5.0V,Io=10mA-1000mA,1us		40		mV
Iocp	Over Current Limit For Output		1700		mA
Vuvp	Under Voltage Int For Output		0.9*Vo		V
Vovp	Over Voltage Int For Output		1.1*Vo		V
Rds(on)	Power Mosfet Switches High-side		240		mΩ
L	External Inductance DCR<50mΩ		4.7		uH
C	External Capacitance ESR<50mΩ		10		uF

Table 4-5 DCDC3 Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
Vi	Input Voltage	3.2	4.1	5	V
Vo	Output Voltage	2.6	3.1	3.3	V
Io	Output Current Drivability ΔVo/Vo=-5%		1000		mA
Fsw	Switching Frequency	0.85	1.6	2.7	MHz
Vripple	Output Ripple Voltage Vo=3.1V,Io=1000mA		10		mV
	Output Ripple Voltage Vo=3.1V,Io=20mA		100		
Eff	Efficiency Vi=3.8V Vo=3.1V,Io=300mA		92		%
Tpu	Power Up Time	30	50	120	us
Tpd	Power Down Time Io=10mA		5		ms
LNR	Line Regulation Vi=3.3V-5.0V,Io=1000mA		0.05		%/V
LDR	Load Regulation Vi=5.0V,Io=10mA-1000mA		0.05		%/A
LDTR	Load Transient Response Vi=5.0V,Io=10mA-1000mA,1us		120		mV
Iocp	Over Current Limit For Output		1950		mA
Vuvp	Under Voltage Int For Output		0.9*Vo		V
Vovp	Over Voltage Int For Output		1.1*Vo		V
Rds(on)	Power Mosfet Switches High-side		270		mΩ
L	External Inductance DCR<50mΩ		2.2		uH
C	External Capacitance ESR<50mΩ		10		uF

4.4 LDO

Table 4-6 LDO1 Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
Vi	Input Voltage	3.2		5	V
Vo	Output Voltage	2.6	3.1	3.3	V
Io	Output Current Drivability ΔVo/Vo=-5%		200		mA
PSRR	Power Supply Restrain Ratio Vi =3.6V, Io=200mA 10kHz		-38		db
Tpu	Power Up Time	600	800	1000	us
Tpd	Power Down Time Io=10mA		2		ms
LNR	Line Regulation Vi=3.3V-5.0V,Io=400mA		0.05		%/V
LDR	Load Regulation Vi=5.0V,Io=10mA-400mA		0.05		%/A
LDTR	Load Transient Response Vi=5.0V,Io=10mA-400mA,1us		75		mV
Iocp	Over Current Protect For Output		900		mA
Vuvp	Under Voltage Protect For Output		2.65		V
Vovp	Over Voltage Protect For Output Vo=3.1V		3.3		V
$V_{drop(min)}$	Min Dropout voltage Io=400mA		200		mV
C	External Capacitance ESR<100mΩ		2.2		uF

Table 4-7 LDO2 Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
Vi	Input Voltage	3.2		5	V
Vo	Output Voltage	2.6	3.1	3.3	V
Io	Output Current Drivability ΔVo/Vo=-5%		200		mA
PSRR	Power Supply Restrain Ratio Vi =3.6V, Io=200mA 10kHz		-42		db
Tpu	Power Up Time	600	800	1000	us
Tpd	Power Down Time Io=10mA		2		ms
LNR	Line Regulation Vi=3.3V-5.0V,Io=200mA		0.05		%/V
LDR	Load Regulation Vi=5.0V,Io=10mA-200mA		0.05		%/A
LDTR	Load Transient Response Vi=5.0V,Io=10mA-200mA,1us		50		mV
Iocp	Over Current Protect For Output		480		mA
Vuvp	Under Voltage Protect For Output		2.65		V
Vovp	Over Voltage Protect For Output Vo=3.1V		3.35		V
$V_{drop(min)}$	Min Dropout voltage Io=200mA		350		mV
C	External Capacitance ESR<100mΩ		2.2		uF

Table 4-8 LDO3 Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
Vi	Input Voltage	3.2		5	V
Vo	Output Voltage	1.5	1.8	2.0	V
Io	Output Current Drivability ΔVo/Vo=-5%		200		mA
PSRR	Power Supply Restrain Ratio Vi =3.6V, Io=200mA 10kHz		-42		db
Tpu	Power Up Time	600	800	1000	us

Tpd	Power Down Time Io=10mA		1		ms
LNR	Line Regulation Vi=3.3V-5.0V,Io=200mA		0.05		%/V
LDR	Load Regulation Vi=5.0V,Io=10mA-200mA		0.05		%/A
LDTR	Load Transient Response Vi=5.0V,Io=10mA-200mA,1us		65		mV
Iocp	Over Current Protect For Output		725		mA
Vuvp	Under Voltage Protect For Output		1.65		V
Vovp	Over Voltage Protect For Output Vo=1.8V		1.95		V
$V_{drop(min)}$	Min Dropout voltage Io=200mA		350		mV
C	External Capacitance ESR<100mΩ		1.0		uF

Table 4-9 LDO5 Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
Vi	Input Voltage	3.2		5	V
Vo	Output Voltage	2.6	2.8	3.3	V
Io	Output Current Drivability ΔVo/Vo=-5%		150		mA
PSRR	Power Supply Restrain Ratio Vi =3.6V, Io=200mA 10kHz		-48		db
Tpu	Power Up Time	600	750	1000	us
Tpd	Power Down Time Io=10mA		1		ms
LNR	Line Regulation Vi=3.3V-5.0V,Io=150mA		0.05		%/V
LDR	Load Regulation Vi=5.0V,Io=10mA-150mA		0.05		%/A
LDTR	Load Transient Response Vi=5.0V,Io=10mA-150mA,1us		30		mV
Iocp	Over Current Protect For Output		380		mA
Vuvp	Under Voltage Protect For Output		2.5		V
Vovp	Over Voltage Protect For Output Vo=2.8V		3.0		V
$V_{drop(min)}$	Min Dropout voltage Io=100mA		350		mV
C	External Capacitance ESR<100mΩ		1.0		uF

Table 4-10 LDO6 Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
Vi	Input Voltage	3.2		5	V
Vo	Output Voltage	0.7	1.2	1.4	V
Io	Output Current Drivability ΔVo/Vo=-5%		200		mA
PSRR	Power Supply Restrain Ratio Vi =3.6V, Io=200mA 10kHz		-44		db
Tpu	Power Up Time	400	550	700	us
Tpd	Power Down Time Io=10mA		1		ms
LNR	Line Regulation Vi=3.3V-5.0V,Io=200mA		0.05		%/V
LDR	Load Regulation Vi=5.0V,Io=10mA-200mA		0.05		%/A
LDTR	Load Transient Response Vi=5.0V,Io=10mA-200mA,1us		35		mV
Iocp	Over Current Protect For Output		510		mA

Vuvp	Under Voltage Protect For Output		1.0		V
Vovp	Over Voltage Protect For Output Vo=1.2V		1.3		V
$V_{drop(min)}$	Min Dropout voltage Io=200mA		350		mV
C	External Capacitance ESR<100mΩ		1.0		uF

Table 4-11 LDO7 Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
Vi	Input Voltage	3.2		5	V
Vo	Output Voltage	1.5	1.8	2	V
Io	Output Current Drivability ∆Vo/Vo=-5%		200		mA
PSRR	Power Supply Restrain Ratio Vi =3.6V, Io=200mA 10kHz		-44		db
Tpu	Power Up Time	400	500	600	us
Tpd	Power Down Time Io=10mA		1		ms
LNR	Line Regulation Vi=3.3V-5.0V,Io=200mA		0.05		%/V
LDR	Load Regulation Vi=5.0V,Io=10mA-200mA		0.05		%/A
LDTR	Load Transient Response Vi=5.0V,Io=10mA-200mA,1us		35		mV
Iocp	Over Current Protect For Output		510		mA
Vuvp	Under Voltage Protect For Output		1.5		V
Vovp	Over Voltage Protect For Output Vo=1.8V		1.9		V
$V_{drop(min)}$	Min Dropout voltage Io=200mA		350		mV
C	External Capacitance ESR<100mΩ		1.0		uF

Table 4-12 LDO11 Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
Vi	Input Voltage	3.2		5	V
Vo	Output Voltage	2.6	3.1	3.3	V
Io	Output Current Drivability ∆Vo/Vo=-5%		30		mA
Tpu	Power Up Time		5		ms
Tpd	Power Down Time Io=10mA		1		ms
LNR	Line Regulation Vi=3.3V-5.0V,Io=30mA		0.05		%/V
LDR	Load Regulation Vi=5.0V,Io=1mA-30mA		0.05		%/A
LDTR	Load Transient Response Vi=5.0V, Io=1mA-30mA, 1us		80		mV
$V_{drop(min)}$	Min Dropout voltage Io=20mA		350		mV
C	External Capacitance ESR<100mΩ		1.0		uF

Table 4-13 LDO12 Parameters

Symbol	Characteristic & Condition	Min	Typ	Max	Units
Vi	Input Voltage	3.2		5	V
Vo	Output Voltage		1.8		V
Io	Output Current Drivability ∆Vo/Vo=-5%		15		mA

Tpu	Power Up Time	100	180	250	us
Tpd	Power Down Time Io=5mA		1		ms
LNR	Line Regulation Vi=3.3V-5.0V,Io=15mA		0.05		%/V
LDR	Load Regulation Vi=5.0V,Io=1mA-15mA		0.05		%/A
LDTR	Load Transient Response Vi=5.0V,Io=1mA-15mA,1us		30		mV
$V_{drop(min)}$	Min Dropout voltage Io=15mA		350		mV
C	External Capacitance ESR<100mΩ		1.0		uF

4.5 Typical Characteristics

4.6 Efficiency Parameter

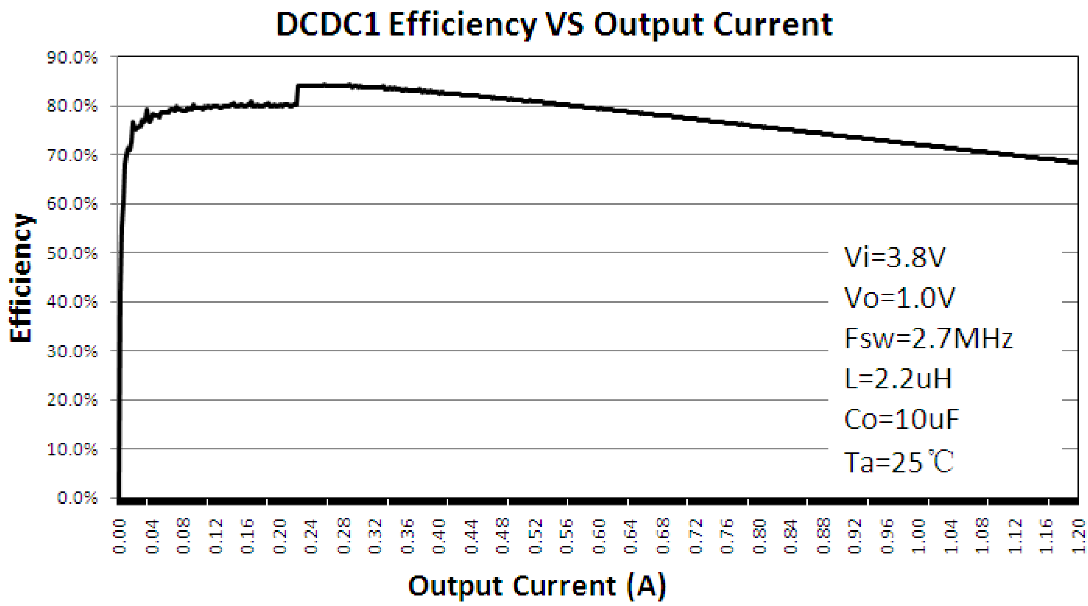


Figure 4-2 DCDC1 Efficiency

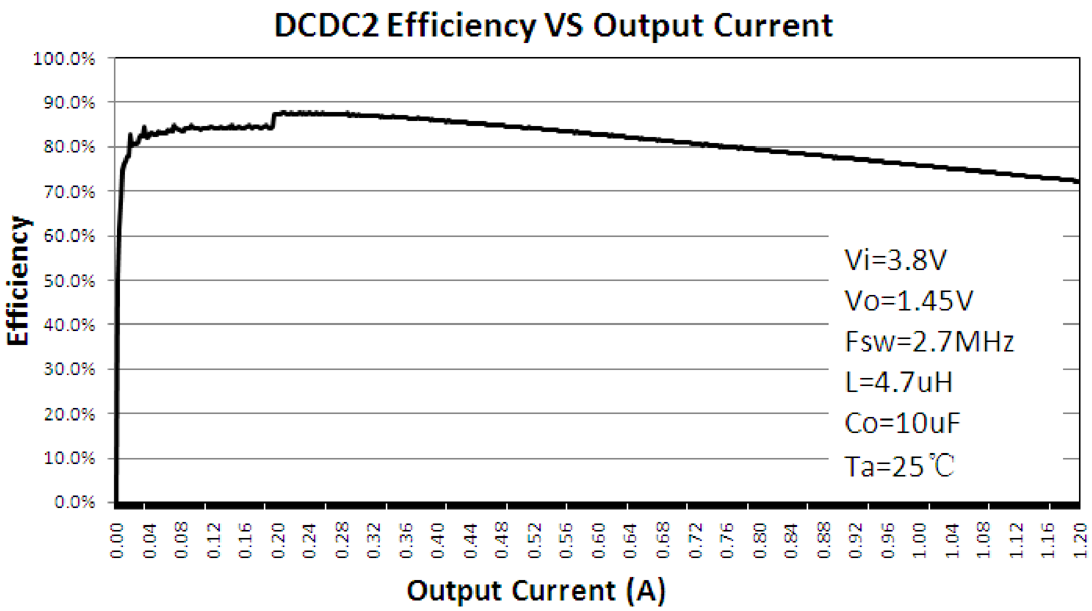


Figure 4-3 DCDC2 Efficiency

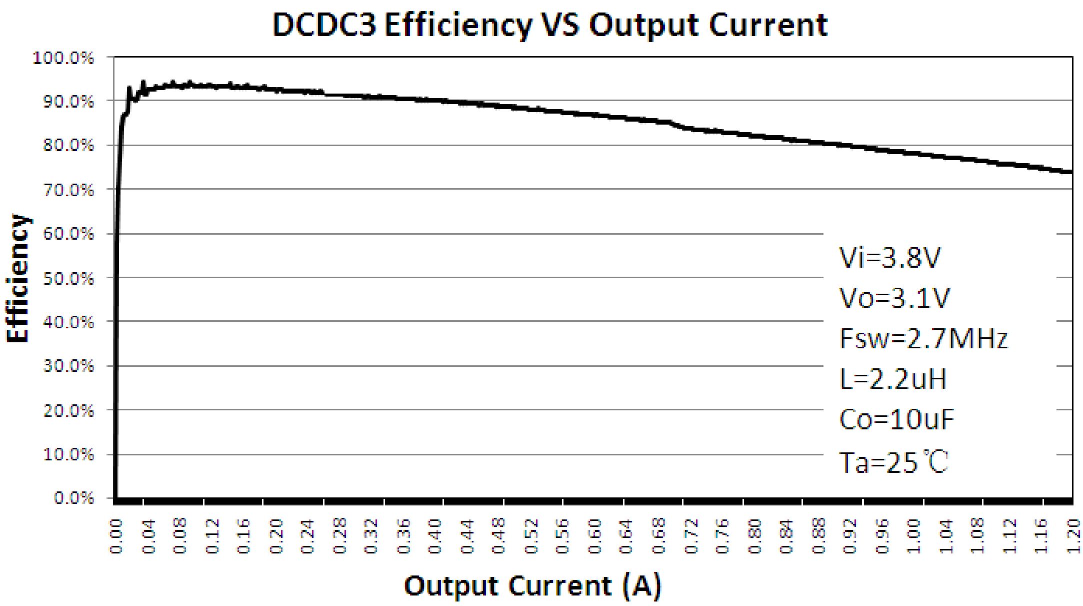


Figure 4-4 DCDC3 Efficiency

4.7 Load Transient Response

Vi=3.8V, Fsw=2.7MHz , 0-80%load ， Tr/Toff=1us , Co=10uF , Unless other Notes 。

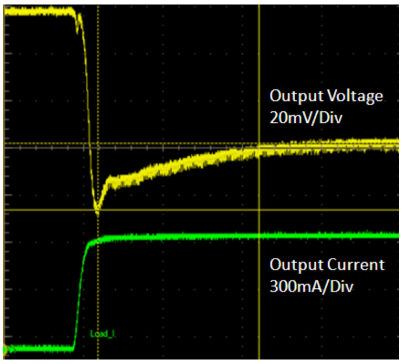


Figure 4-5 DCDC1 Load Transient Response

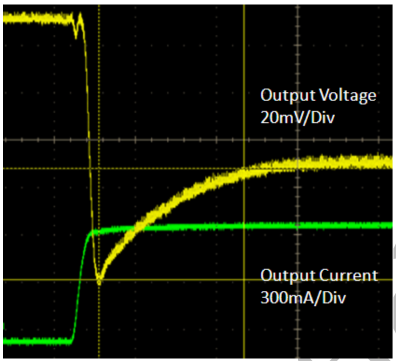


Figure 4-6 DCDC2 Load Transient Response

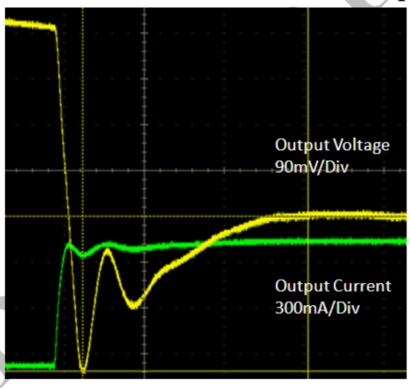


Figure 4-7 DCDC3 Load Transient Response

5 Audio Codec Subsystem

5.1 Audio Diagram

Audio Codec subsystem integrates I2S interface, DAC, ADC, AGC interface, MIC amplifier, FM amplifier and headphone PA. I2S interface in slave mode supports 2.0 channel transmitter and receiver. I2S supports sample rate of 192k/96k/48k/32k/24k/16k/12k/8k/88.2k/44.1k/22.05k/11.025k. The 2.0 channel Sigma-Delta DAC supports the same sample rate as I2S. The stereo 20mW PA (Power Amplifier) is integrated for headphone with 41-level volume and mute control, Non-direct and Direct Drive mode both with anti-pop circuit are supported for headphone. The subsystem supports stereo analog microphones (AMIC). The AMIC interface provides programmable bias output. There are configurable Automatic Gain Control (AGC), Zero Crossing and Noise gating for analog microphone.

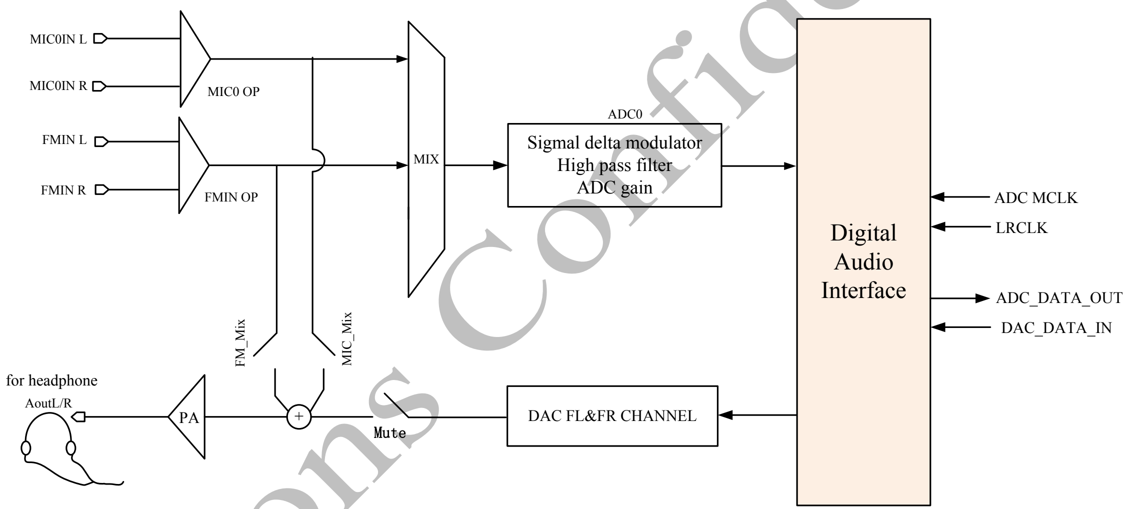


Figure 5-1 Audio Diagram & Signal Path

5.1.1 Register List

Table 5-1 AUDIO OUT IN Controller Registers Address

Name	Physical Base Address
AUDIO_OUT	0xA0
AUDIO_IN	0xA0

Table 5-2 Audio Registers

Offset	Register Name	Description
0x0	AUDIOINOUT_CTL	AUDIO IN/OUT Control for I2S Register
0x2	DAC_DIGITALCTL	DAC Control EN&MUTE Register
0x3	DAC_VOLUMECTL0	DAC FL&FR VOLUME Control Register

0x4	DAC_ANALOG0	DAC Analog 0 Register
0x5	DAC_ANALOG1	DAC Analog 1 Register
0x6	DAC_ANALOG2	DAC Analog 2 Register
0x7	DAC_ANALOG3	DAC Analog 3 Register
0x8	ADC_DIGITALCTL	ADC0 Digital Control Register
0x9	ADC_HPFCTL	ADC0 High Pass Filter Control Register
0xA	ADC_CTL	ADC0 control register
0xB	AGC_CTL0	AGC0 Control 0 Register
0xC	AGC_CTL1	AGC0 Control 1 Register
0xD	AGC_CTL2	AGC0 Control 2 Register
0xE	ADC_ANALOG0	ADC Analog 0 Register
0xF	ADC_ANALOG1	ADC Analog 1 Register

5.1.2 Register Description

5.1.2.1 AUDIOINOUT_CTL

AUDIO IN/OUT Control for I2S Register
Offset = 0x00

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11	MDD	MCLK Divided to DAC 0:DIV=1 1:DIV=2	RW	0
10	HIOID	headset or earphone INOUT detect IRQ enable 0: disable 1: enable	RW	0
9	OCIEN	Direct Drive Output Over Current status IRQ 1: enable 0: disable If DAC_ANALOG2[5] is enabled and DAC_ANALOG3[14] is high, when this bit is enabled, an interrupt will be sent to the interrupt controller.	RW	0
8	OEN	I2S Output Enable. 0: Disable 1: Enable	RW	0
7	-	Reserved	-	-
6:5	IMS	I2S RX&TX Mode Select 00:3 wires mode 01:4 wires mode 10:6 wires mode 11:Reserved	RW	00
4:0	-	Reserved	-	-

5.1.2.2 DAC_DIGITALCTL

DAC Control EN_MUTE Register
Offset = 0x02

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	RW	0
11:10	DACINSEL	DAC input source select 00:I2S0(music) 01: Reserved 10: Reserved 11: Reserved	RW	00
9	DEDFL_FR	DACFL&FR EN_DITH 1:Enable 0:Disable	RW	0
8	DISRS	DAC INPUT SAMPLE RATE SEL 0:MCLK/256 1:MCLK/128	RW	0
7:6	DBWFL_FR	DACFL&FR BANDWIDTH 00:Wide 01:Middle 10:Narrow 11:Reserved	RW	00
5:4	DOSRSFL_FR	DAC FL&FR OUTPUT SAMPLE RATE SEL 00:MCLK/16 01:MCLK/8 10:MCLK/4 11:MCLK/2	RW	00
3	DMFR	DACFR DIGITAL MUTE 1:Mute 0:Unmute	RW	0
2	DMFL	DACFL DIGITAL MUTE 1:Mute 0:Unmute	RW	0
1	DEFR	DACFR DIGITAL ENABLE 1:Enable 0:Disable	RW	0
0	DEFL	DACFL DIGITAL ENABLE 1:Enable 0:Disable	RW	0

5.1.2.3 DAC_VOLUMECTL0

DAC FL_FR VOLUME CONTROL ((3/8) dB/level)
Offset = 0x03

Bit(s)	Name	Description	Access	Reset

15:8	DACFR_VOLUME	VOLUME CONTROL (3/8) dB/level 0xFF :+24 dB …… 0xBF : 0 dB 0xBE : -3/8 dB …… 0x00 : -72 dB	RW	BE
7:0	DACFL_VOLUME	VOLUME CONTROL (3/8) dB/level 0xFF :+24 dB …… 0xBF : 0 dB 0xBE : -3/8 dB …… 0x00 : -72 dB	RW	BE

5.1.2.4 DAC_ANALOG0

DAC Analog Register
Offset = 0x04

Bit(s)	Name	Description	Access	Reset
15:14	PAIB	PA bias current control. 11:biggest 00:smallest	RW	01
13:12	OPDAVB	OPDA bias voltage control. 11:biggest 00:smallest	RW	01
11	-	Reserved	-	-
10:8	OPDAIB	OPDA bias current control. 111:biggest 000:smallest	RW	011
7:6	OPDTSIB	OPDTS bias current control. 11:biggest 00:smallest	RW	01
5:4	OPVBIB	OPVB bias current control. 11:biggest 00:smallest	RW	01
3	-	Reserved	-	-
3	KFEN	Karaoke Mix Function Enable 0:disable 1:enable *Note: when enable this bit, MIC0INL and MIC0INR will be added and transmitted to PA*	RW	0
2:0	OPGIB	OPG bias current control.	RW	101

		111:biggest 000:smallest		

5.1.2.5 DAC_ANALOG1

DAC Analog Register
Offset = 0x05

Bit(s)	Name	Description	Access	Reset
15	MICMUTE	MIC mute, 0: mute 1: Unmute	RW	0
14	FMMUTE	FM mute, 0: mute 1: Unmute	RW	0
13:11	-	Reserved	-	-
10	DACFL_FRMUTE	DACFL&FR Playback Mute 0: mute DAC Playback, 1: enable DAC playback	RW	0
9:8	PAIQ	PA output stage IQ control. 00:smallest 11:biggest	RW	00
7	ZERODT	Zero data for DAC analog part 0:disable, 1:enable	RW	0
6	PASW	PA output swing select. 0:2.828Vpp 1:1.6Vpp This bit will control the attenuation before DAC's output goes into PA. Set this bit to 1 when PA is driving a headphone, there must to be attenuation for DAC's output (from about 2.4Vpp to 1.6Vpp) and PA will output 1.6Vpp at max volume. Set it to 0, there will be no attenuation and PA will output 2.4Vpp and can function as LINEOUT.	RW	1
5:0	VOLUME	Headphone Amp Volume Control. 41 levels in total (Values between 0b000000 and 0b101000 are valid. Any value over 0b101000 set to it will be taken as 0b101000 actually. Reading value will just show what you have written to it.)	RW	000000

5.1.2.6 DAC_ANALOG2

DAC Analog2 Register

Offset = 0x06

Bit(s)	Name	Description	Access	Reset
15	PAZD	PA Output Volume Near Zero Detect: 0:Invalid 1:Valid When this bit is selected 1, "click" of volume tuning will cut down. But if small volume is selected, this bit should be 0 to avoid some issue.	RW	0
14:12	-	Reserved	-	-
11	DACI	DAC Current select: 0:Small 1:Large	RW	0
10	P2IB	PA bias Double for ATP2 mode: 0: *1 1: *2	RW	0
9	ATP2CE	For ATP2,On-chip ramp Connect EN: 0: Disconnect 1: Connect	RW	0
8	PAVDC	Antipop2 PA discharge control: 0: switch open 1: switch closed, discharge	RW	0
7	FLRADD	FML add FMR to PAL and PAR 0: disable 1: enable	RW	0
6	PAMIX	DAC to PA output mix configure: 0: not mix 1:DACFL+DACFR to AOUTFL and AOUTFR	RW	0
5	DDOVV	Direct Drive overload protect and recover 0: Overload protect and recover is valid 1: Overload protect and recover is invalid	RW	0
4	OPVROEN	Analog circuit of the internal DAC_OPVRO enable 0: Disable 1: Enable	RW	0
3	DDATPR	Direct Drive antipop_VRO Resistant Connect Enable: 0: disconnect 1: connect	RW	0
2:0	OPVROOSIB	Analog circuit of the internal DAC_OPVRO output stage IQ control. 111:biggest 000:smallest	RW	000

5.1.2.7 DAC_ANALOG3

DAC Analog3 Register
Offset = 0x07

Bit(s)	Name	Description	Access	Reset
15	-	Reserved	-	-
14	OVLS	DAC VRO overload state: 1: VRO overload 0: VRO normal working state	R	0
13	VLCHD	Volume change Delay bit: 0: disable 1: enable	RW	0
12:11	-	Reserved	-	-
10	BIASEN	All DAC&PA Bias enable 0: disable 1: enable	RW	0
9	ATPLP2_FR_FL	Channel FR&FL Antipop2 LOOP2 enable 0: disable 1: enable	RW	0
8:7	OPCM1IB	OPCM1 bias current control. 11:biggest 00:smallest	RW	01
6:4	OPVROIB	OPVRO bias current control. 000:smallest 111:biggest	RW	011
3	PAOSEN_FR&FL	PA FR&FL output stage enable 0: disable 1: enable	RW	0
2	PAEN_FR&FL	PA FR&FL enable 0: disable 1: enable	RW	0
1	DACEN_FL	DAC FL ANALOG enable 0: disable 1: enable	RW	0
0	DACEN_FR	FR DAC ANALOG enable 0: disable 1: enable	RW	0

5.1.2.8 ADC_DIGITALCTL

ADC0 Digital Control Register
Offset=0x08

Bits	Name	Description	Access	Reset
15:13	-	Reserved	-	-

12	ADCOS	ADC OUTPUT SELECT 0: I2S OUTPUT 1: Reserved	RW	0
11	AD0LR	ADC0L And ADC0R Added enable 0: disable 1: enable Note: this bit is designed for karaoke use, when this bit is 1, ADC0L data and ADC0R data are added and transmitted to MCU.	RW	0
10	-	Reserved	-	-
9:6	ADGC0	ADC0 DIGITAL Gain Control 0000: 0dB 0001: 3dB 0010: 6dB 0011: 9dB 0100: 12dB 0101: 15dB 0110: 18dB 0111: 21dB 1000: 24dB 1001: 27dB 1010: 30dB 1011: 33dB 1100: 36dB 1101: 39dB 1110: 42dB 1111: 45dB	RW	0000
5:0	-	Reserved	-	-

5.1.2.9 ADC_HPFCTL

ADC Digital Control Register

Offset=0x09

Bits	Name	Description	Access	Reset
15:8	-	Reserved	-	-
7:6	SRSEL0	SR select for removing wind noise filter0 00:8kHz/11.025kHz/12kHz 01:16kHz/22.05kHz/24kHz 10:32kHz/44.1kHz/48kHz 11:Reserved	RW	00

<table>
<tr><td>5:3</td><td>WNHPF0CUT</td><td>Wind Noise filter0 Cut Off frequency settings:
<table>
<tr><td></td><td colspan="9">SR fs(kHz)</td></tr>
<tr><td></td><td>8</td><td>11.025</td><td>12</td><td>16</td><td>22.05</td><td>24</td><td>32</td><td>44.1</td><td>48</td></tr>
<tr><td>000</td><td>82</td><td>113</td><td>122</td><td>82</td><td>113</td><td>122</td><td>82</td><td>113</td><td>122</td></tr>
<tr><td>001</td><td>102</td><td>141</td><td>153</td><td>102</td><td>141</td><td>153</td><td>102</td><td>141</td><td>153</td></tr>
<tr><td>010</td><td>131</td><td>180</td><td>196</td><td>131</td><td>180</td><td>196</td><td>131</td><td>180</td><td>196</td></tr>
<tr><td>011</td><td>163</td><td>225</td><td>245</td><td>163</td><td>225</td><td>245</td><td>163</td><td>225</td><td>245</td></tr>
<tr><td>100</td><td>204</td><td>281</td><td>306</td><td>204</td><td>281</td><td>306</td><td>204</td><td>281</td><td>306</td></tr>
<tr><td>101</td><td>261</td><td>360</td><td>392</td><td>261</td><td>360</td><td>392</td><td>261</td><td>360</td><td>392</td></tr>
<tr><td>110</td><td>327</td><td>450</td><td>490</td><td>327</td><td>450</td><td>490</td><td>327</td><td>450</td><td>490</td></tr>
<tr><td>111</td><td>408</td><td>563</td><td>612</td><td>408</td><td>563</td><td>612</td><td>408</td><td>563</td><td>612</td></tr>
</table></td><td>RW</td><td>000</td></tr>
<tr><td>2</td><td>HPF0DW</td><td>Select High Pass Filter0 for DC offset or Wind Noise
0: for DC offset
1: for Wind Noise</td><td>RW</td><td>0</td></tr>
<tr><td>1</td><td>HPF0LEN</td><td>High Pass Filter0 L Enable
0: enable
1: disable</td><td>RW</td><td>0</td></tr>
<tr><td>0</td><td>HPF0REN</td><td>High Pass Filter0 R Enable
0: enable
1: disable</td><td>RW</td><td>0</td></tr>
</table>

5.1.2.10 ADC_CTL

ADC control register
Offset=0x0A

Bits	Name	Description	Access	Reset
15	-	Reserved	-	-
14	FMLEN	FM input left channel enable; 0: Disable 1: Enable	RW	0
13	FMREN	FM input right channel enable; 0: Disable 1: Enable	RW	0
12:10	FMGAIN	FM input gain control: 000:-3.0dB 001:-1.5dB 010:0.0dB 011:1.5dB 100:3.0dB 101:4.5dB 110:6.0dB 111:7.5dB	RW	010
9:8	-	Reserved	-	-

7	MIC0LEN	MIC0 input L Channel Enabled 0: disable 1: enable	RW	0
6	MIC0REN	MIC0 input R Channel Enabled 0: disable 1: enable	RW	0
5	MIC0FDSE	MIC0 input Fully differential or Single ended select 0: Fully Differential; 1: Single Ended;	RW	0
4	AD0LEN	ADC0 Left Channel Enable 0: disable 1: enable	RW	0
3	AD0REN	ADC0 Right Channel Enable 0: disable 1: enable	RW	0
2	ATAD	PA OUT TO ADC ENABLE 0: disable 1: enable	RW	0
1:0	MTA	MIC TO ADC ENABLE 0: disable 1: enable	RW	0

5.1.2.11 AGC_CTL0

AGC0 Control Register 0
Offset = 0x0B

Bits	Name	Description	Access	Reset

15:12	AMP1G0L	AMP1 Left Channel Gain Select at AGC0 disabled 0000: 16.5dB 0001: 18.0dB 0010: 19.5dB 0011: 21.0dB 0100: 22.5dB 0101: 24.0dB 0110: 25.5dB 0111: 27.0dB 1000: 28.5dB 1001: 30.0dB 1010: 31.5dB 1011: 33.0dB 1100: 34.5dB 1101: 36.0dB 1110: 37.5dB 1111: 39.0dB AMP1 AGC Gain can be Read out when AGC0 is enabled, and can be written and read out when AGC0 is disabled.	RW	1001
11:8	AMP1G0R	AMP1 Right Channel Gain Select at AGC0 disabled 0000: 16.5dB 0001: 18.0dB 0010: 19.5dB 0011: 21.0dB 0100: 22.5dB 0101: 24.0dB 0110: 25.5dB 0111: 27.0dB 1000: 28.5dB 1001: 30.0dB 1010: 31.5dB 1011: 33.0dB 1100: 34.5dB 1101: 36.0dB 1110: 37.5dB 1111: 39.0dB AMP1 AGC Gain can be Read out when AGC0 is enabled, and can be written and read out when AGC0 is disabled.	RW	1001
7	IMICSHD	Internal MIC Power Controlled by External MIC Plug enable 0: disable 1: enable	RW	0

6	VMICEXEN	External MIC Power VMIC enabled 0: disabled 1: enabled	RW	0
5:4	VMICEXST	External MIC Power VMIC voltage setting 00 2.7V 01 2.9V 10 3.1V 11 3.2V	RW	1
3	VMICINEN	Internal MIC Power VMIC Control 0:disable 1:enable	RW	0
2:0	AMP0GR1	AMP1 Gain Boost Range Select 000: +3.0dB 001: +6.0dB 010: +9.0dB 011: +12.0dB 100: +13.5dB 101: +15.0dB 110: +16.5dB 111: +18.0dB	RW	011

5.1.2.12 AGC_CTL1

AGC0 Control 1 Register
Offset=0x0C

Bits	Name	Description	Access	Reset
15:14	VCDL	headset input current detect level (μA) 00:50 01:100 10:150 11:200	RW	0x3
13	MIS	headset input state 0:not input 1:input	R	0
12:10	NGT0	AGC0 Noise gate statistic time, (SCY = 1.36ms) 000: 4*SCY 001: 8*SCY 010: 16*SCY 011: 32*SCY 100: 64*SCY 101: 128*SCY 110: 256*SCY 111: 512*SCY	RW	001

9:7	ATKT0	AGC0 Attack(Gain ramp-down) Time for every Gain step, (SCY = 683µs) 000: 1*SCY 001: 2*SCY 010: 4*SCY 011: 8*SCY 100: 16*SCY 101: 32*SCY 110: 64*SCY 111: 128*SCY	RW	010
6:4	DCYT0	AGC0 Decay(Gain ramp-up) Time for every Gain step, (SCY = 5.46ms) 000: 16*SCY 001: 32*SCY 010: 64*SCY 011: 128*SCY 100: 256*SCY 101: 512*SCY 110: 1024*SCY 111: 2048*SCY	RW	001
3:2	CMR0	AGC0 RC filter cutoff frequency select 00:207Hz 01: 414Hz 10: 828Hz 11: 1.65kHz	RW	10
1:0	SCY0	AGC0 sense Cycle select 00 :341µs 01: 683µs 10 :1366µs 11 :2732µs	RW	10

5.1.2.13 AGC_CTL2

AGC Control 2 Register
Offset=0x0D

Bits	Name	Description	Access	Reset
15:13	TARGL0	AGC0 AMP1 Target level select at AMP2GR=+6dB 000: -42dBFS 001: -39dBFS 010: -36dBFS 011: -33dBFS 100: -30dBFS 101: -27dBFS 110: -24dBFS 111: -21dBFS	RW	100

12:10	NGTHSEL0	AGC0 Noise Gate Threshold select at +28.5dB Gain (Peak sense) 000: -27dBFS 001: -30dBFS 010: -33dBFS 011: -36dBFS 100: -39dBFS 101: -42dBFS 110: -45dBFS 111: -51dBFS	RW	011
9	MICAAEN	ADC0 MIC to PA Path differential compensation enable 0: Disable 1: Enable	RW	0
8	-	Reserved	-	-
7	RMSINSEL0	AGC0 input source select 0: Left 1: Right	RW	0
6	MGE	MIC gain 0dB enable 0:disable 1:enable	RW	0
5	NGSLEN0	AGC0 Noise Gate maintain current Gain or keep silence 0: maintain current Gain 1: keep silence	RW	0
4	NGTEN0	AGC0 Noise Gate function enable 0: disabled 1: enabled	RW	0
3	ZEROC0	AGC0 Gain change at zero-cross enabled 0: disabled 1: enabled	RW	0
2	GREN0	AGC0 Gain_con gain reset function enable 0: disabled 1: enabled	RW	0
1	AGC0LEN	AGC0 Left channel Enable 0: disabled 1: enabled	RW	0
0	AGC0REN	AGC0 Right channel Enable 0: disabled 1: enabled	RW	0

5.1.2.14 ADC_ANALOG0

ADC Analog 0 Register

Offset=0x0E

Bits	Name	Description	Access	Reset

15:13	IVSRMSTN	IVSRMS bias tune 000: -25% 001: -18.75% 010: -12.5% 011: -6.25% 100: 0% (Baseline value 2μA) 101: +6.25% 110: +12.5% 111: +18.75%	RW	100
12:11	EICDL	Earphone input current dectec level (mA) 00:0.9 01:1.0 10:1.1 11:1.2	RW	0
10:9	EHOCDL	Earphone or headset out current detect level (μA) 00:10 01:20 10:30 11:40	RW	1
8	EIS	Earphone input state 0:NOT INPUT 1:INPUT	R	0
7: 5	OPBC1	The bias current select for OPAD1 in A/D: 000: 3μA 001: 4μA 010: 5μA 011: 6μA 100: 7μA 101: 8μA 100: 9μA 110: 10μA 111: 11μA	RW	011
4:3	OPBC23	The bias current select for OPAD2/3 in A/D: 00: 2μA 01: 3μA 10: 4μA 11: 5μA	RW	01
2:0	VRDABC	Audio A/D Voltage Reference bias current select: 000: 2μA 001: 3μA 010: 4μA … 110: 8μA 111: 9μA	RW	001

5.1.2.15 ADC_ANALOG1

ADC Analog 1 Register
Offset=0x0F

Bits	Name	Description	Access	Reset
15:13	LPFBC	Audio A/D LPF bias current select: 000: 3.0μA 001: 3.5μA 010: 4.0μA 011: 4.5μA 100: 5.0μA 101: 5.5μA 110: 6.0μA 111: 6.5μA	RW	100
12:11	LPFBUFBC	FD LPF BUF OP bias current select: 00: 4μA 01: 5μA 10: 6μA 11: 7μA	RW	01
10	ADCBIAS	ADC Total Bias Tune 0: Normal 1: +50%	RW	0
9	-	Reserved	-	-
8	HIDE	headset or earphone input detect enable 0 :disable 1 :enable	RW	1
7:6	FD1BC	MIC Preamp FDOP1 bias current select : 00: 3μA 01: 4μA 10: 5μA 11: 6μA	RW	01
5:4	FD2BC	MIC Preamp FDOP2 bias current select : 00: 2μA 01: 3μA 10: 4μA 11: 5μA	RW	01
3:2	FD1BUFBC	MIC Preamp FDOP2 bias current select : 00: 2μA 01: 3μA 10: 4μA 11: 5μA	RW	01

1:0	FMBC	FM Pre-amplifiers bias current select: 00: 3μA 01: 4μA 10: 5μA 11: 6μA	RW	01

5.2 Audio Characteristics

The audio characteristics are measured under the following conditions:
AVCC = 2.9V, VCC = 3.1V, VDD = AVDD = 1.8V, Vref = 1.5V.
When testing DAC+PA or PA, a 16Ohm or 32Ohm load resistor is applied.

5.2.1 DAC+PA

Table 5-3 DAC + Direct Drive PA characteristics

Characteristics	Min	Typ	Max	Unit
Noise		12		μV
SNR		93.3		dB
SNR(A-Weighting)		96.8		dB
Dynamic Range (-48dB Input)		95		dB
Dynamic Range (A-Weighting, -48dB Input)		98		dB
THD+N (0dB Input)		-85		dB
Max Ampl (0dB Input)		588		mV
Max Power		20.6		mW
Interchannel Isolation (1kHz, 0dB sine wave Input)		-82dB /-82dB (L mute/R mute)		dB

Table 5-4 DAC + Non-Direct Drive PA @FS=48K characteristics

Characteristics	Min	Typ	Max	Unit
Noise		11.5		μV
SNR		96		dB
SNR(A-Weighting)		98.5		dB
Dynamic Range (-48dB Input)		94		dB
Dynamic Range (A-Weighting, -48dB Input)		97		dB
THD+N (0dB Input)		-85		dB
Max Ampl (0dB Input)		575		mV
Max Power		20.2@220μF		mW
Interchannel Isolation (1kHz, 0dB Sine wave Input)		-86dB/-84dB (L mute/R mute)		dB

Figure 5-2 shows the frequency Response of DAC @ INPUT AMP = 0dB & load = 16R:

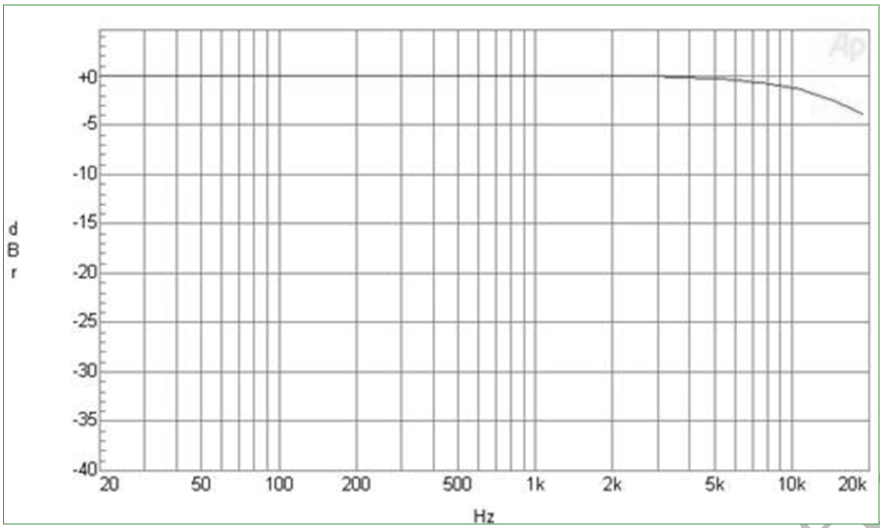


Figure 5-2 Frequency Response of DAC

Figure 5-3 below gives the FFT spectrum of DAC @ INPUT AMP = 0dB & 1 kHz:

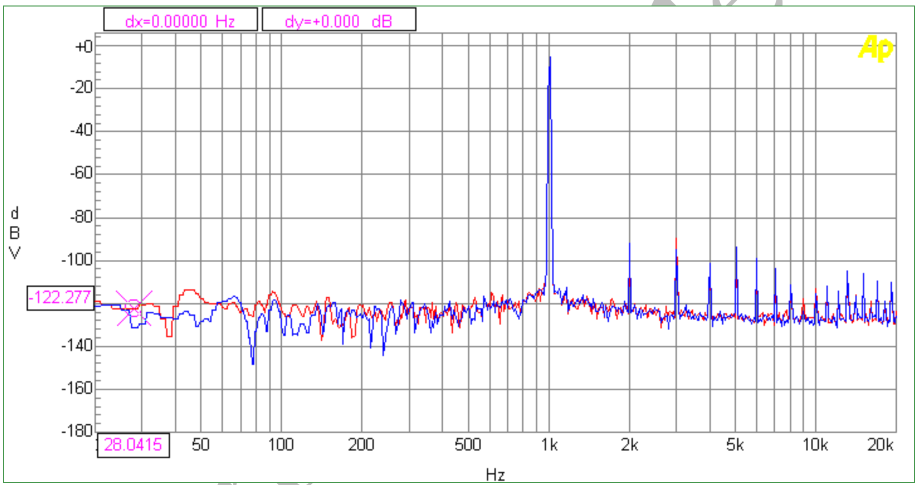


Figure 5-3 DAC FFT response

5.2.2 PA

Table 5-5 Non-Direct Drive PA characteristics

Characteristics	Min	Typ	Max	Unit
Noise		14		μV
SNR		93.5		dB
Dynamic Range		93		dB
THD+N		-82		dB
Output Common Mode Voltage		1.505		Vrms
Full Scale Output Voltage@-60dB THD+N		0.650Vrms(2Vpp)		Vrms
Output Power @16.5Ohm		25mW		mW

Figure 5-4 below is the frequency Response of the Non-direct Drive PA @1.6Vpp input:

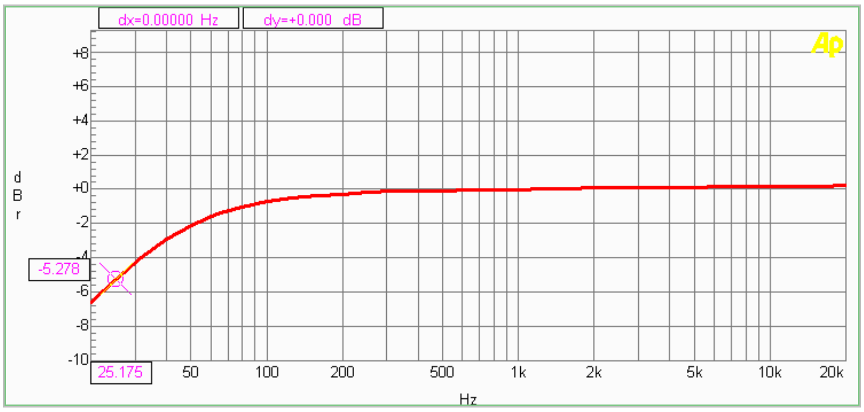


Figure 5-4 Frequency Response

Figure 5-5 gives the THD+N vs. INPUT AMP Curve of the Non-direct Drive PA:

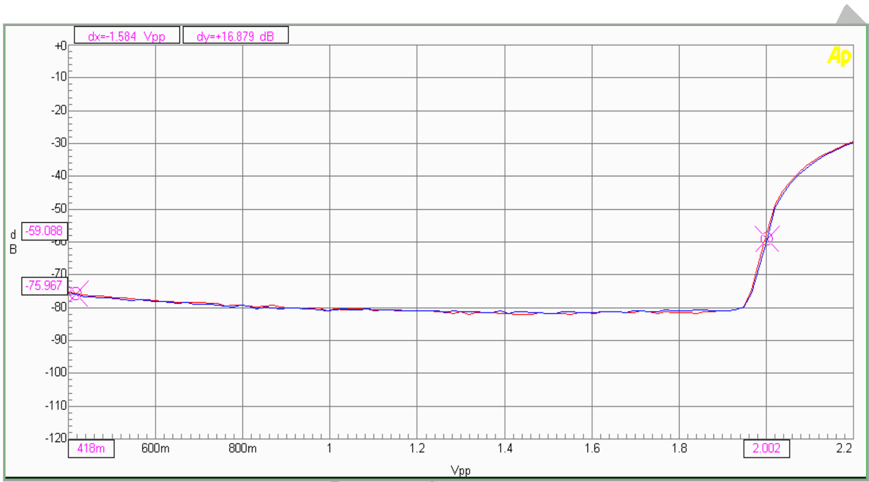


Figure 5-5 THD+N vs. INPUT AMP Curve

Table 5-6 Direct Drive PA Characteristics

Characteristics	Min	Typ	Max	Unit
Noise		16		µV
SNR		92.3		dB
Dynamic Range		92.1		dB
THD+N		-81	-78	dB
Output Common Mode Voltage		1.5		Vrms
Full Scale Output Voltage@-60dB THD+N		0.660Vrms(2Vpp)		Vrms
Output Power @16Ohm		26		mW

Figure 5-6 below is the Frequency Response of Direct Drive PA @1.6Vpp input:

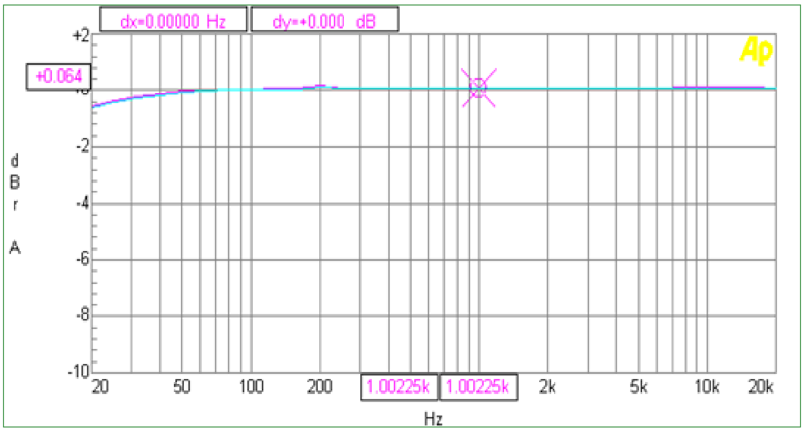


Figure 5-6 Frequency Response

Figure 5-7 is the THD+N vs. INPUT AMP Curve of the Direct Drive PA:

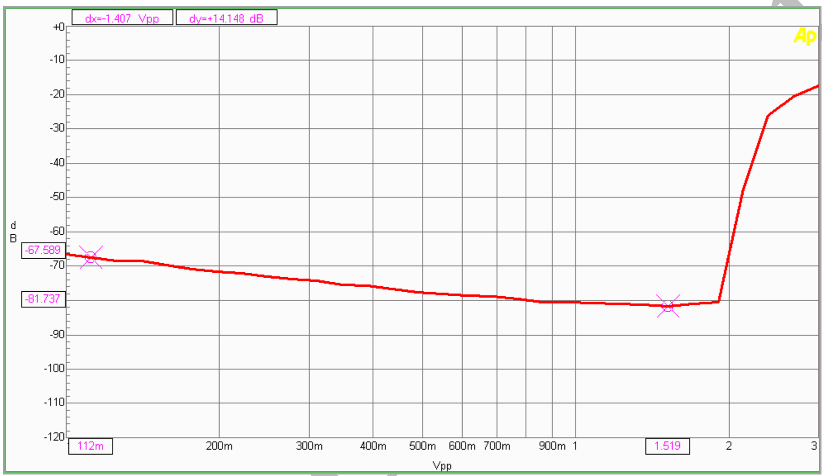


Figure 5-7 THD+N vs. Input AMP

5.2.3 ADC

Table 5-7 ADC characteristics

Test condition: Temp =25°C, AVCC = 3.0V, VCC = 1V, VDD = AVDD = 1.8V, Vref = 1.5V @2Vpp, 1 kHz, sine wave input

Characteristics	Min	Typ	Max	Unit
Dynamic Range (–40 dBFS Input), unweighting		91		dB
Dynamic Range (–40 dBFS Input), weighting		92.7		dB
THD+N, unweighting		-85		dB
THD+N, weighting		-87.5		dB

6 TWI Interface

6.1 Features

ATC2603C can be accessed by Master through a standard TWI (Two-Wire Interface), which allows Master to write commands to and read status from ATC2603C by accessing its registers. TWI only occupies two pins namely SCL (Serial Clock) and SDA (Serial Data), information is transmitted serially on SDA and clock is driven on SCL by Master. ATC2603C is a slave device controlled by Master, The transmission speed of TWI interface supports 400Kbps, 8-bit address and 16-bit data width with MSB transmitted first. The default slave address is 0xCA.

A typical sequence of Writing 16-bit data to a register is shown in the Figure below. A start bit is generated by Master, followed by a slave address, then register address and 16-bit data. A SACK acknowledge signal will be given by ATC2603C after every byte address or data transmission. The transmission stops when Master sends a stop bit. All the 16-bit data should be written before the register is updated.

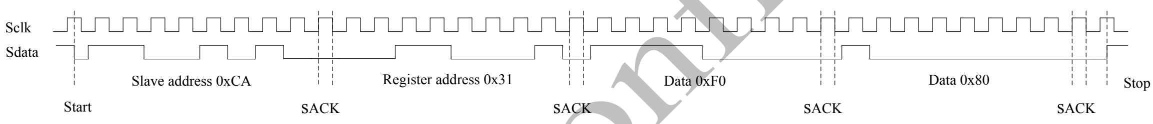


Figure 6-1 Writing 16-bit data to register through TWI bus

The Figure above shows a sequence of writing a 16-bit data 0xF080 to register 0x31, the slave address is 0xCA.

A typical 16-bit data read sequence is shown below. Firstly, Master writes slave address and register address to ATC2603C. Then a start bit and the slave address is sent indicating a read sequence started. In the following 8-bit clock, Master reads data from ATC2603C, during which Master sends a MACK signal every 8-bit data or address, mNACK signal will be sent to ATC2603C to stop the reading process, then Master generates a stop bit indicating the reading is completed.

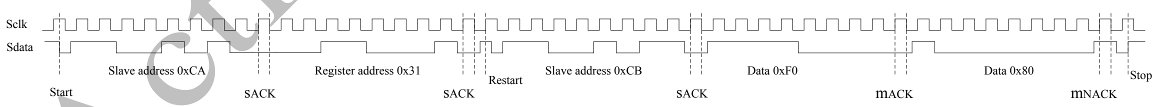


Figure 6-2 Reading 16-bit data from register through TWI bus

The Figure above illustrates Master reads 16-bit data 0xF080 from register 0x31, the slave address is 0xCA.

6.2 Register List

Table 6-1 TWI Interface Register Block Address

Block Name	Base Address
TWSI_REGISTER	0xF8

Table 6-2 TWI Register Offset

Offset	Register Name	Description
0x08	SADDR	TWI serial interface slave device register

6.3 Register Description

6.3.1 SADDR

Two-Wire Serial interface slave device address register
Offset = 0x08

Bit(s)	Name	Description	Access	Reset
15:8	-	Reserved	-	-
7:1	SDA	Slave device address The register contains the slave device address used in slave mode.	RW	0x65
0	FCS	Filter pulse Cycle select 0: filter 2 cycles noise(83.3ns) 1: filter 1cycle noise(41.7ns)	RW	0

7 Power Management Unit

7.1 Features

The highly integrated Power Management Unit (PMU) in ATC2603C provides a full solution for the single cell lithium battery power system, the communication with Master is done through TWI interface. PMU consists of 3 DC-DCs, 9 LDOs (one of which is SWITCH-LDO), 10-bit multiplex ADC, one linear charging-management unit, fuel gauge, and self-adaption power distribution control unit etc, automatically monitoring abnormal power conditions like overvoltage, overcurrent, undervoltage and overtemperature, etc.

The linear charging-management unit for Li-Ion battery adjusts the charging current automatically according to the battery's status, including trickle, CC (Constant Current) and CV (Constant Voltage) charging phase, with maximum charging current of 2A. Furthermore, it also supports overcharge protection and timeout protection, etc.

Self-Adaption Power Distribution (APDS) control module is an integrated unit inside PMU, which controls the power distribution and seamless power switching among BAT, VBUS and WALL to guarantee a stable power supply for the whole system. The minimum Standby current can be lower than 30μA. The input voltage of integrated 10-bit, 16-channel Analog-to-Digital converter (AuxADC) ranges from 0V to 3V, is used for detecting the voltage, current and temperature.

7.2 Module Description

7.2.1 DC-DC Module

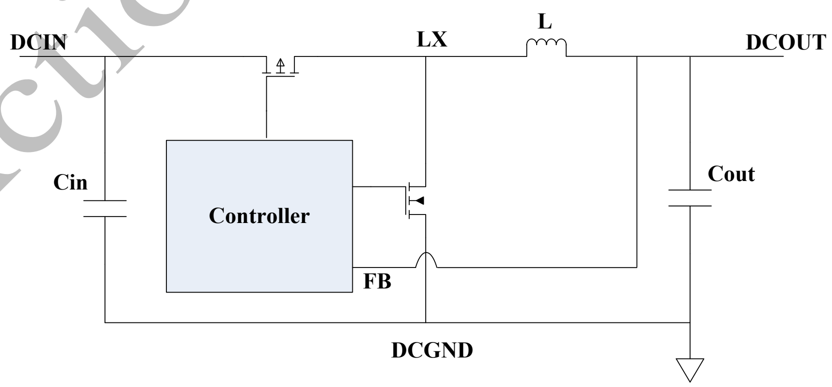


Figure 7-1 ATC2603C Buck DC-DC circuit diagram

ATC2603C integrates 3 Buck DC-DCs: DC-DC1, DC-DC2 and DC-DC3. All the 3 Buck DC-DCs are synchronized controlled and integrates internal MOSFET. For normal application, one inductor and two capacitors should be applied outside. The key parameters and recommended components selection is listed in Table 7-1 below.

Table 7-1 Key parameters and External components selection for DC-DCs

Buck	Vin (V)	Vout (V)	Adjustable Voltage Step (mV)	Imax (A)	L	Cin/Cout	Application
DC-DC1	3.3~5.5	0.7~1.4	25	1.2	2.2µH(DCR <0.05Ohm)	10µF/20µF	Master core
DC-DC2	3.3~5.5	1.3~2.15	50	1	2.2µH(DCR <0.05Ohm)	10µF/20µF	DDR
DC-DC3	3.3~5.5	2.6~3.3	100	1	4.7µH(DCR <0.1Ohm)	10µF/20µF	Master/ATC2603C IO

Note: the maximum current of DC-DC3 is 800mA when working without inductance.

The Efficiency characteristics of these DC-DCs are shown in Figure 7-2

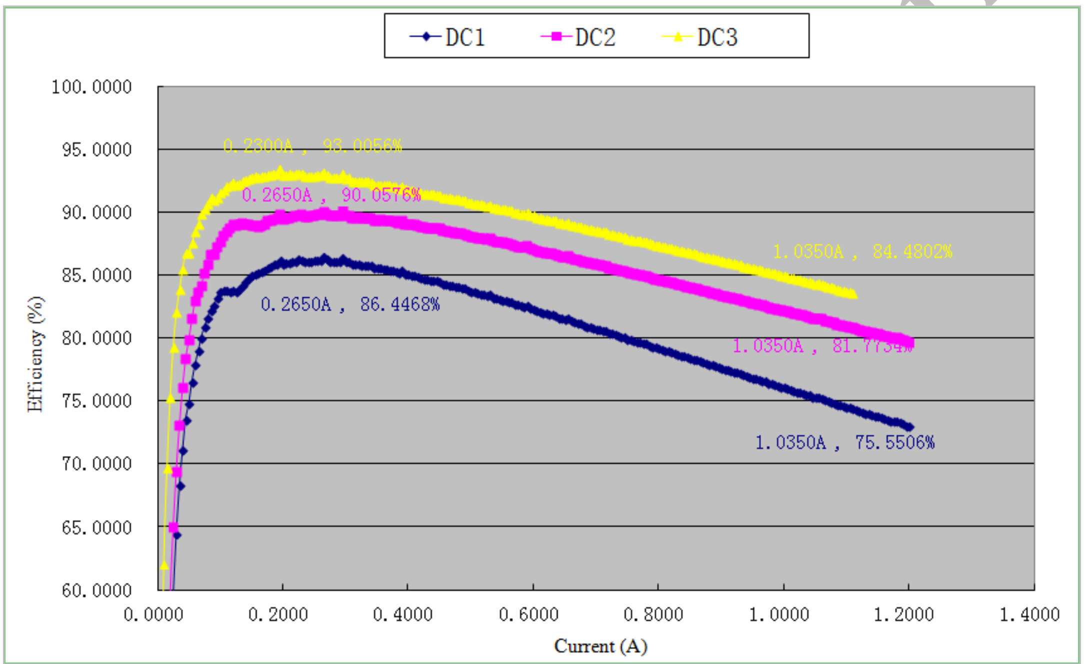


Figure 7-2 ATC2603C Buck DC-DCs Efficiency curve

7.2.2 LDO Module

ATC2603C integrates 9 LDOs in total, their specifications are listed below in Table 7-2. LDO support output overvoltage, overcurrent and undervoltage protection. Whenever the output voltage exceeds the overvoltage range, LDOs will generate an overvoltage interrupt, besides, the LDOs overvoltage protection can be enabled or disabled through the relevant register. Overcurrent and Undervoltage are the same mechanism.

Table 7-2 LDO regulators specifications

Regulator	Vin (V)	Vout(V)	Imax(mA)	Cin(µF)	Cout(µF)	Application Reference
LDO1	3.0~5.5	2.6~3.3	200	0.1	2.2	Sensor2V8
LDO2	3.0~5.5	2.6~3.3	200	0.1	2.2	Master/ATC2603C

						AVCC
LDO3	3.0~5.5	1.5~2.0	250	0.1	2.2	ATCVDD1V8
LDO5	3.0~5.5	2.6~3.3	150	0.1	2.2	TPVCC
LDO6	3.0~5.5	0.7~1.4	200	0.1	2.2	Master AVDD
LDO7	3.0~5.5	1.5~2.0	200	0.1	2.2	Sensor1V8
LDO11	3.0~5.5	2.6~3.3	25	0.1	1.0	SVCC
LDO12	3.0~5.5	1.5~2.0	15	0.1	1.0	RTCVDD
SWITCH-LDO	-	-	400	-	-	SD Card

Note1: LDO12 output voltage is dependent with supply voltage and is not adjustable. The relationship between LDO3 and LDO12 is not fixed, LDO3 voltage is register adjustable.

Note2: when SWITCH-LDO is configured to SWITCH mode, the output voltage equals the input voltage; when SWITCH-LDO is configured as LDO, the output voltage ranges 3.0~3.3V, and its input is tied internally.

7.2.3 Charger Module

ATC2603C integrates one constant current and constant voltage charger, providing battery detection, trickle current charging and it can adjust the charging current according to system power consumption. When an external adaptor is plugged in, the battery's existence is detected by ATC2603C PMU according to the voltage on BAT PIN, once SYSPWR is detected higher than battery voltage (VBAT), the charger will be enabled by software and ATC2603C PMU will manage the charging process automatically. Charging current can be configured through register (max 2A) and the real-time charging current can be read by the ADC charging current register.

The IC internal temperature and battery temperature are monitored throughout the charging process, once the temperature is detected higher or lower than the standard value, an interrupt signal will be sent, and software will take measures then charging process will be paused. The battery's temperature is measured by the circuit shown in Figure 7-3 below.

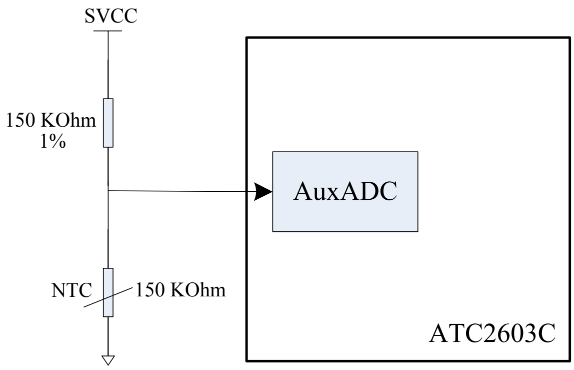


Figure 7-3 ATC2603C Battery Temperature Detecting Diagram

7.2.4 APDS Module

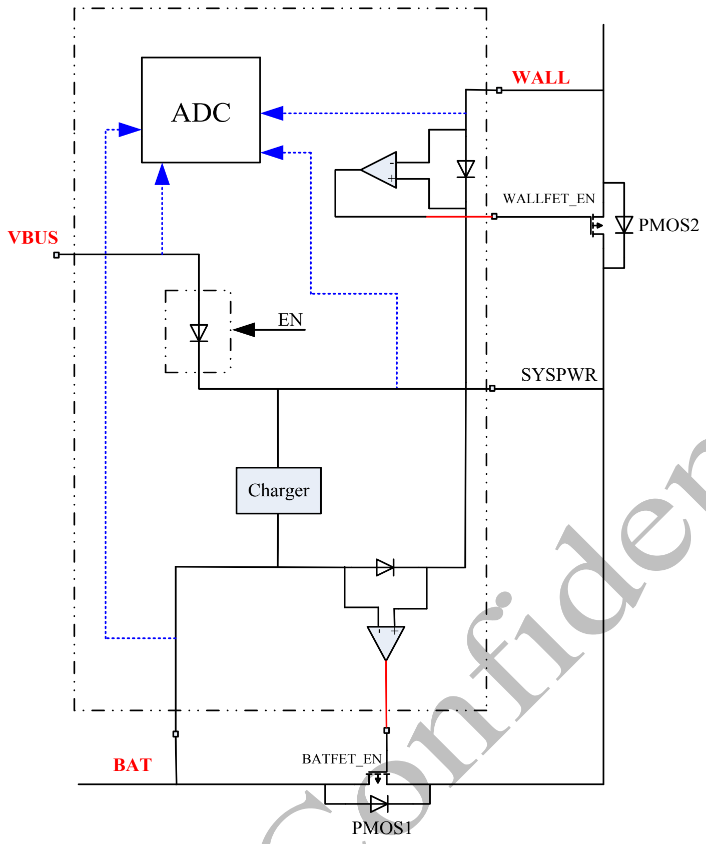


Figure 7-4 APDS Module Diagram

ATC2603C APDS (Adaptive Power Distribute System) block diagram (for CHIP_VER(0xDC)=0x0) is shown in Figure 7-4 above. SYSPWR is a public power supply node for all the DC-DCs and LDOs. PMU gets power from BAT, VBUS and WALL and then supplies to the public node SYSPWR through a diode respectively in the IC. To prevent current from flowing from VBUS to SYSPWR in OTG application, an enable control pin (EN) is applied to the diode between VBUS and SYSPWR. When this diode is disabled, the path from BUS to SYSPWR will be cut off completely. PMU needs to supply high power, in order to reduce internal thermal dissipation, two external MOSFET PMOS1 and PMOS2 are applied to bypass big current, see in Figure 7-4 above.

Note that for CHIP_VER(0xDC)=0x1, the diode is replaced by a LDO, the mechanism is identical.

Voltages on BAT, VBUS, WALL and SYSPWR nodes as well as the current flows through each diode are monitored since the system is powered on. Once the output voltage of BAT exceeds the upper or lower limits, PMU will send BAT overvoltage or undervoltage interrupt to INTS module. When the current through BAT path is detected higher than the set value, a BAT overcurrent interrupt will be sent to INTS module, what's more, if this current exceeds overcurrent shut-off value, the power will be forced to shut off to protect IC. If VBUS and WALL are detected overvoltage, undervoltage or overcurrent, the same process will be triggered as BAT does.

7.2.5 Power Modes

According to the application, the following 4 types of power modes are distinguished:

- **S1-Working Mode**: In Working Mode, Master can work normally including its kernel and IOs, that is to say, DC-DC1 and DC-DC3 needed by the Master and ATC2603C must work properly. LDO1, LDO2, LDO3, LDO6, LDO11, LDO12 and their related control logic circuits should work. Other regulators can be either on or off. This state is called S1.
- **S2-Standby Mode**: Both Master IC's kernel and IOs are shut off in this mode, DC-DC1, DC-DC3, LDO1, LDO2, LDO3 and LDO6 are powered off accordingly, LDO11 and LDO12 is still on. Essential information is saved in DDR for fast start-up, so DC-DC2 should work normally. The communication between Master and ATC2603C is disabled. We called this state S2.
- **S3-Sleep Mode**: When the device is not used for a long time, the system will enter S3 state, which is a low power state. In this case, DDR will be power down, but SYSPWR still supplies the system. Only LDO11 and LDO12 is on, others are all power off.
- **S4-Deep Sleep Mode**: In this mode, the power consumption is reduced more deeply than standby mode, LDO11 is power down, and only LDO12 is on.

Wakeup elements:

The system can be woke up in different conditions, which involves several wake up elements including ONOFF, ALARM, SGPIOIRQ, RESET, REM_CON, USB, WALL, HDSW, IR. In S2 and S3, each of the elements above can wake up the system. In S4, SVCC is shut off, only RTCVDD exists, so only SGPIOIRQ, REM_CON and IR cannot wake up the system, others can wake up the system. Either long or short press on ONOFF button can wake up the system, which can be enabled or disabled by the register. In S1 mode, the system can be configured into S2, S3 or S4 by software, setting the related bits EN_S1, EN_S2, EN_S3, shown in Table 7-3 below.

Table 7-3 Power State changed by Software

Power State	EN_S1	EN_S2	EN_S3
S4	0	0	0
S3	0	0	1
S2	0	1	x
S1	1	x	x

Note: When the system need to go into S2 from S1, set EN_S2=1 first, then write 0 to EN_S1, to switch the system from S1 mode to S2.

Overcurrent protection:

If one of the LDOs is overcurrent, and overcurrent interrupt is sent, PWROK will be pulled down first, and then it will enter Standby state by setting EN_S2 and EN_S3.

If overcurrent is detected on BAT, WALL or VBUS, and its overcurrent shut off function is enabled, then it will entering Standby state according to the settings of EN_S2 and EN_S3.

Overtemperature protection:

When the temperature in IC exceeds the settings, and its overtemperature protection is enabled, then the system will enter Standby state by setting EN_S2 and EN_S3 automatically.

7.2.6 POR and Power ON/OFF Sequence Module

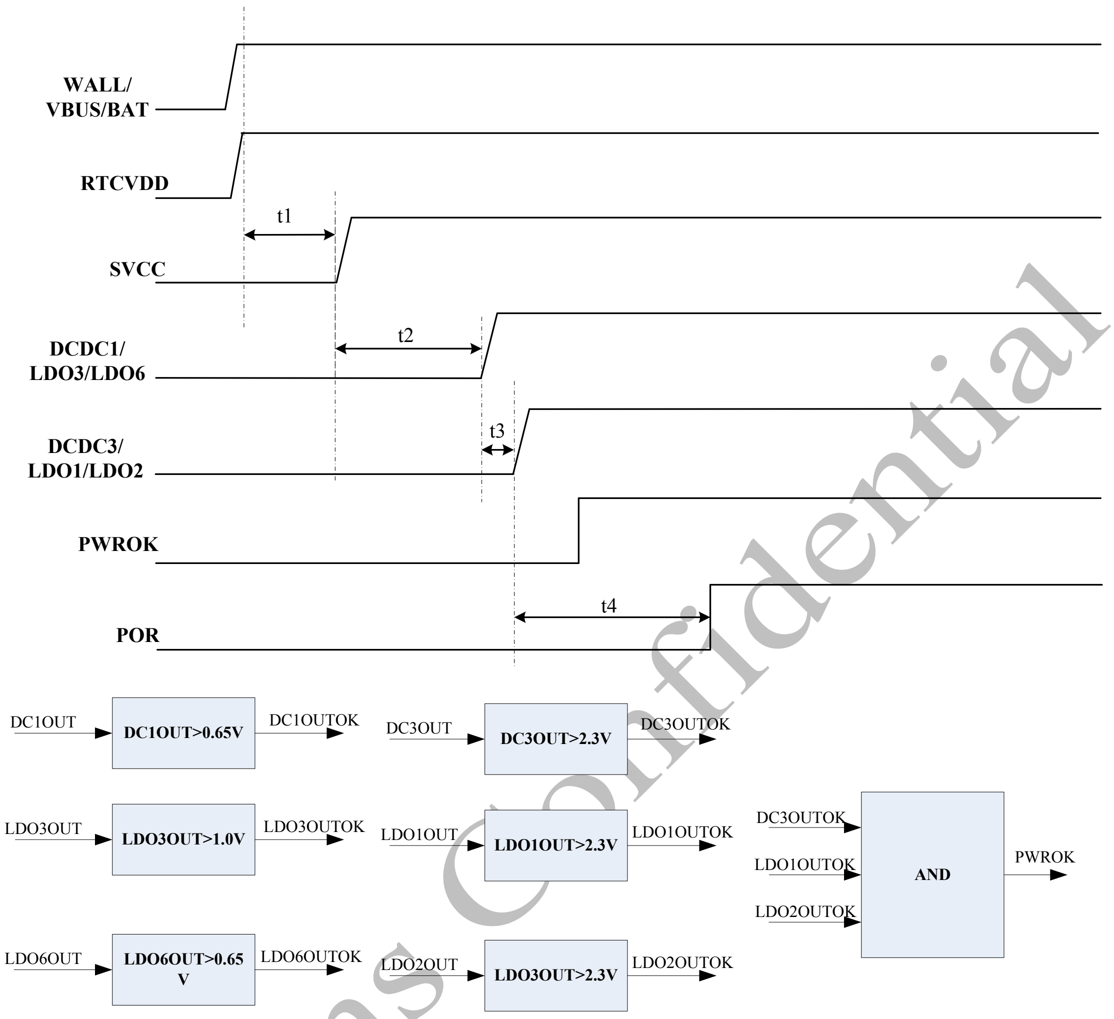


Figure 7-5 Power on Sequence

Figure 7-5 above shows ATC2603C power on sequence, the power of BAT or WALL or VBUS is turned on firstly, RTCVDD and SVCC will be generated closely after that. Then ATC2603C's core voltage (1.8V) and Master's core voltage (1.0V) will be applied. The high-voltage supply for ATC2603C and Master will be generated afterwards. At last, when all these power is stable, the POR signal will be sent to Master, which indicates the Master starts to run. The timing parameter is of power on sequence is listed in Table 7-4 below.

Table 7-4 Timing Parameter of Power on Sequence

Parameter	Tmin(ms)	Tmax(ms)
t1	35.6	81.3
t2	26.1	72.7
t3	2.4	6.2
t4	33.8	92.5
DC-DC3 to LDO1 and LDO1 to LDO2	0	0.12

If the system is set to power down by software, Master will send commands to ATC2603C, on

receiving the commands, ATC2603C will pull down PWROK and POR, then shut off DC-DC1, DC-DC3, LDO1, LDO2, LDO3 and LDO6.
If system is force to power down, then if any of DC1OUTOK, DC3OUTOK, LDO1OUTOK, LDO2OUTOK, LDO3OUTOK or LDO6OUTOK is detected high to low, ATC2603C will pull POR down immediately.

7.2.7 ONOFF & Reset Module

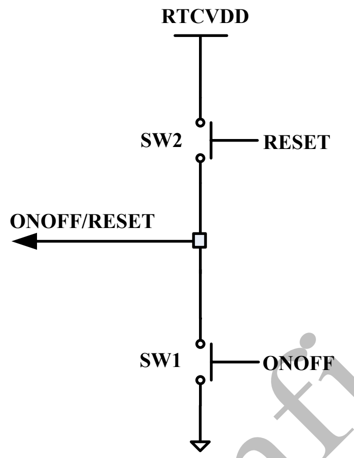


Figure 7-6 ONOFF & Reset Module Diagram

In the PMU, ONOFF and Reset multiplex one PIN (ONOFF/RESET), shown in figure 7-6. Either ONOFF or RESET button is pressed down, SYSRST or SYSONOFF signal will be high and generates a trigger to PMU through ONOFF/RESET pin accordingly. If the RESET and ONOFF buttons are pressed down at the same time, all the registers in RTCVDD voltage domain will be reset. Long press on ONOFF button for more than a setting period (6s, 8s, 10s or 12s) will trigger a same function like P_RESET to reset the whole system.

7.2.8 PWM Module

PWM module get the divided clock by register PWMCLKDIV from Master, and there are two PWM modules, PWM0 and PWM1, which can be used for breath light control.

7.3 Register List

Table 7-5 PMU Block Address

Name	Base Address
PMU	0x00

Table 7-6 PMU Controller Registers

Offset	Register Name	Description
0x00	PMU_SYS_CTL0	PMU SYSTEM CONTROL Register0

0x01	PMU_SYS_CTL1	PMU SYSTEM CONTROL Register1
0x02	PMU_SYS_CTL2	PMU SYSTEM CONTROL Register2
0x03	PMU_SYS_CTL3	PMU SYSTEM CONTROL Register3
0x04	PMU_SYS_CTL4	PMU SYSTEM CONTROL Register4
0x05	PMU_SYS_CTL5	PMU SYSTEM CONTROL Register5
0x0A	PMU_BAT_CTL0	PMU BAT CONTROL Register0
0x0B	PMU_BAT_CTL1	PMU BAT CONTROL Register1
0x0C	PMU_VBUS_CTL0	PMU VBUS CONTROL Register0
0x0D	PMU_VBUS_CTL1	PMU VBUS CONTROL Register1
0x0E	PMU_WALL_CTL0	PMU WALL CONTROL Register0
0x0F	PMU_WALL_CTL1	PMU WALL CONTROL Register1
0x10	PMU_SYS_PENDING	PMU SYSTEM Pending Register
0x11	PMU_DC1_CTL0	PMU DC-DC1 CONTROL Register0
0x14	PMU_DC2_CTL0	PMU DC-DC2 CONTROL Register0
0x17	PMU_DC3_CTL0	PMU DC-DC3 CONTROL Register0
0x1E	PMU_LDO1_CTL	PMU LDO1 CONTROL Register
0x1F	PMU_LDO2_CTL	PMU LDO2 CONTROL Register
0x20	PMU_LDO3_CTL	PMU LDO3 CONTROL Register
0x22	PMU_LDO5_CTL	PMU LDO5 CONTROL Register
0x23	PMU_LDO6_CTL	PMU LDO6 CONTROL Register
0x24	PMU_LDO7_CTL	PMU LDO7 CONTROL Register
0x28	PMU_LDO11_CTL	PMU LDO11 CONTROL Register
0x29	PMU_SWITCH_CTL	PMU SWITCH CONTROL Register
0x2A	PMU_OV_CTL0	PMU OVER VOLTAGE CONTROL Register0
0x2B	PMU_OV_CTL1	PMU OVER VOLTAGE CONTROL Register1
0x2C	PMU_OV_STATUS	PMU OVER VOLTAGE Status Register
0x2D	PMU_OV_EN	PMU OVER VOLTAGE Detect ENABLE Register
0x2E	PMU_OV_INT_EN	PMU OVER VOLTAGE INT ENABLE Register
0x2F	PMU_OC_CTL	PMU OVER CURRENT CONTROL Register
0x30	PMU_OC_STATUS	PMU OVER CURRENT Status Register
0x31	PMU_OC_EN	PMU OVER CURRENT Detect ENABLE Register
0x32	PMU_OC_INT_EN	PMU OVER CURRENT INT ENABLE Register
0x33	PMU_UV_CTL0	PMU UNDER VOLTAGE CONTROL Register0
0x34	PMU_UV_CTL1	PMU UNDER VOLTAGE CONTROL Register1
0x35	PMU_UV_STATUS	PMU UNDER VOLTAGE Status Register
0x36	PMU_UV_EN	PMU UNDER VOLTAGE Detect ENABLE Register
0x37	PMU_UV_INT_EN	PMU UNDER VOLTAGE INT ENABLE Register
0x38	PMU_OT_CTL	PMU OVER TEMPERTURE CONTROL Register
0x39	PMU_CHARGER_CTL0	PMU CHARGER CONTROL Register0
0x3A	PMU_CHARGER_CTL1	PMU CHARGER CONTROL Register1
0x3B	PMU_CHARGER_CTL2	PMU CHARGER CONTROL Register2
0x3D	PMU_APDS_CTL	PMU APDS CONTROL Register

0x50	PMU_ICMADC	PMU ICMADC Register
0x62	PMU_ABNORMAL_STATUS	PMU Abnormal_Status Register
0x63	PMU_WALL_APDS_CTL	PMU WALL_APDS_CTL
0x64	PMU_REMCON_CTL0	PMU REMCONADC wake up control Register
0x65	PMU_REMCON_CTL1	PMU REMCONADC interrupt control Register
0x66	PMU_MUX_CTL0	PMU MUX CTL0 Register
0x67	PMU_SGPIO_CTL0	PMU SGPIO CTL0 Register
0x68	PMU_SGPIO_CTL1	PMU SGPIO CTL1 Register
0x69	PMU_SGPIO_CTL2	PMU SGPIO CTL2 Register
0x6A	PMU_SGPIO_CTL3	PMU SGPIO CTL3 Register
0x6B	PMU_SGPIO_CTL4	PMU SGPIO CTL4 Register
0x6C	PWMCLK_CTL	PWM clock controller register
0x6D	PWM0_CTL	PWM0 control register
0x6E	PWM1_CTL	PWM1 control register

7.4 Register Description

7.4.1 PMU_SYS_CTL0

PMU_SYS_CTL0 Register (RTCVDD) (default 0xE04B)
Offset = 0x00

Bit(s)	Name	Description	Access	Reset
15	USB_WK_EN	VBUS wake up enable, when exceeds the threshold voltage 1:VBUS can wake up 0:VBUS can't wake up	RW	0x1
14	WALL_WK_EN	WALL wake up enable, when exceeds the threshold voltage 1:WALL can wake up 0:WALL can't wake up	RW	0x1
13	ONOFF_LONG_WK_EN	ONOFF long press wake up enable 1:ONOFF can wake up 0:ONOFF can't wake up	RW	0x1
12	ONOFF_SHORT_WK_EN	ONOFF short press wake up enable 1:ONOFF can wake up 0:ONOFF can't wake up	RW	0x0
11	SGPIOIRQ_WK_EN	SGPIOIRQ wake up enable 1: SGPIOIRQ can wake up 0: SGPIOIRQ can't wake up	RW	0x0
10	RESTART_EN	Restart enable 1:enable 0:default	RW	0x0

		The default value is 0, when it is set to 1(If WALL/VBUS exists, WALL/VBUS wakeup will be HW disabled), the system will enter Standby Mode, then wakes up automatically 2sec later, this bit will be cleared to 0 at the same time.		
9	REM_CON_WK_EN	REM_CON button pressed wake up enable 1:Rem_con can wake up 0:Rem_con can't wake up	RW	0x0
8	ALARM_WK_EN	Alarm wake up enable 1:Alarm can wake up 0:Alarm can't wake up	RW	0x0
7	HDSW_WK_EN	Hard switch wake up enable 0:No 1:Yes	RW	0x0
6	RESET_WK_EN	P_Reset and ONOFF long press Reset wake up enable 0:No 1:Yes This bit can be reset by RTCVDDOK only	RW	0x1
5	IR_WK_EN	IRwake up enable 0:No 1:Yes	RW	0x0
4:3	VBUS_WK_TH	VBUS wake up threshold voltage 00:4.05V 01:4.20V 10:4.35V 11:4.50V	RW	1
2:1	WALL_WK_TH	WALL wake up threshold voltage 00:4.05V 01:4.20V 10:4.35V 11:4.50V	RW	1
0	ONOFF_MUXKEY_EN	ONOFF multiplex enable 0:Disable (No P_RESET key) 1:Enable (With P_RESET key)	RW	0x1

7.4.2 PMU_SYS_CTL1

PMU_SYS_CTL1 Register (RTCVDD) (default 0x000E)
Offset = 0x01

Bit(s)	Name	Description	Access	Reset
15	USB_WK_FLAG	VBUS wakeup flag 1:VBUS wakeup 0:No VBUS wakeup	R	0x0

14	WALL_WK_FLAG	WALL wakeup flag 1:WALL wakeup 0:No WALL wakeup	R	0x0
13	ONOFF_LONG_WK_FLAG	ONOFF long press wakeup flag 1:ONOFF long press wakeup 0:No ONOFF long press wakeup	R	0x0
12	ONOFF_SHORT_WK_FLAG	ONOFF short press wakeup flag 1:ONOFF short press wakeup 0:No ONOFF short press wakeup	R	0x0
11	SGPIOIRQ_WK_FLAG	SGPIOIRQ wakeup flag 1: SGPIOIRQ wakeup 0: No SGPIOIRQ wakeup	R	0x0
10	ONOFF_PRESS_Reset_IRQ_PD	ONOFF_PRESS_Reset interrupt pending bit: 1: ONOFF_PRESS_Reset Interrupt occurs; 0: no ONOFF_PRESS_Reset Interrupt *Note:only for CHIP_VER(0xDC)=0X1*	R	0x0
9	REM_CON_WK_FLAG	REM_CON wakeup flag 1: REM_CON wakeup 0: No REM_CON wakeup	R	0x0
8	ALARM_WK_FLAG	Alarm wakeup flag 1:Alarm wakeup 0: No Alarm wakeup	R	0x0
7	HDSW_WK_FLAG	HDSW wakeup flag 1:HDSW wakeup 0: No HDSW wakeup	R	0x0
6	RESET_WK_FLAG	reset wakeup flag 1:Reset wakeup 0: No reset wakeup	R	0x0
5	IR_WK_FLAG	IR wakeup flag 1:IR wakeup 0: No IR wakeup	R	0x0
4:3	LB_S4	Low power state enter S4 voltage setting 00:2.9V 01:3.0V 10:3.1V 11:3.3V When the system is in S1, S2, S3 and the relative transition state, if the Battery voltage is lower than settings and there is no VBUS and WALL detected, the system enters S4 directly.	RW	0x1
2	LB_S4_EN	Low Power state enter S4 enable (including detection enable) 0:Disable	RW	0x1

		1:Enable		
1	ENRTCOSC	Internal 32kHz clock enable 0:disable 1:enable	RW	0x1
0	EN_S1	Enter S1state enable 0:Do not enter S1 1:Enter S1	RW	0x0

7.4.3 PMU_SYS_CTL2

PMU_SYS_CTL2 Register (RTCVDD) (default 0x0680)
Offset = 0x02

Bit(s)	Name	Description	Access	Reset
15	ONOFF_PRESS	ONOFF key is pressed or not 0:ONOFF key is not pressed 1:ONOFF key is pressed	R	0x0
14	ONOFF_SHORT_PRESS	ONOFF short press pending 0:No ONOFF short press happen 1: ONOFF short press happen Write 1 clear to 0	RW	0x0
13	ONOFF_LONG_PRESS	ONOFF long press pending 0:No ONOFF long press happen 1:ONOFF long press happen Write 1 clear to 0	RW	0x0
12	ONOFF_INT_EN	ONOFF interrupt enable 0:disable 1:enable	RW	0x0
11:10	ONOFF_PRESS_TIME	ONOFF key press time settings **00:** 60ms < t < 0.5s; judged as short press; t >= 0.5s, judged as long press; **01:** 60ms < t < 1s, judged as short press; t >= 1s, judged as long press; **10:** 60ms < t < 2s, judged as short press; t >= 2s, judged as long press; **11:** 60ms < t < 4s, judged as short press; t >= 4s, judged as long press;	RW	0x01
9	ONOFF_PRESS_Reset_EN	ONOFF long press Reset&preset enable: 0:disable;	RW	0x1

		1:enable		
8:7	ONOFF_RESET_TIME_SEL	Long press ONOFF send Reset time selection 00:6s 01:8s 10:10s 11:12s	RW	0x01
6	S2_TIMER_EN	S2 timer enable 0:Disable 1:Enable When 2timer is enabled, once the system enters S2 state, S2timer starts to count, when it counts up the system will enter S3 or S4 state.	RW	0x0
5:3	S2TIMER	S2timer 000:6min 001:16min 010:31min 011:61min 100:91min 101:121min 110:151min 111:181min	RW	0x0
2	ONOFF_PRESS_PD	ONOFF key press happen pending 0:No ONOFF key press happen 1:ONOFF key press happen Write 1 clear to 0	RW	0x0
1	ONOFF_PRESS_INT_EN	ONOFF button pressed for 32ms interrupt enable 0:disable 1:enable	RW	0x0
0	PMU_A_EN	PMU simulation acceleration mode enable 0:diasble 1:enable	RW	0x0

7.4.4 PMU_SYS_CTL3

PMU_SYS_CTL3 Register (RTCVDD) (default 0x0080)

Offset = 0x03

Bit(s)	Name	Description	Access	Reset
15	EN_S2	Enter S2 state enable 0:do not enter S2	RW	0x0

		1:enter S2		
14	EN_S3	Enter S3 state enable 0:do not enter S3 1:enter S3	RW	0x0
13	S3_TIMER_EN	S3 timer enable 0:Disable 1:Enable If S3 timer is enabled, when the system enters S3 state, S3 timer starts to count, when it counts up, the system will enter S4 state.	RW	0x0
12:10	S3TIMER	S3timer 000:6min 001:16min 010:31min 011:61min 100:91min 101:121min 110:151min 111:181min	RW	0x0
9	S2S3TOS1TIMER_EN	When S2/S3 receives the wakeup signal, enable delay of entering S1 from S2/S3 0:disable, no delay from S2/S3 to S1 1:enable, delay for a while from S2/S3 to S1	RW	0
8:7	S2S3TOS1TIMER	When S2/S3 receives the wakeup signal, delay time setting of switching from S2/S3 to S1 00: 3ms 01: 6ms 10: 12ms 11: 24ms	RW	1
6:4	-	Reserved	-	-
3	USBS2OUT_WK_EN	VBUS pull out wakeup enable in S2 mode 0:disable 1:enable When this bit is enabled, if VBUS if pulled out, working mode will be switched from S2 to S1. The wakup voltage of pull out operation is PMU_SYS_CTL0[4:3]	RW	0
2	WALLS2OUT_WK_EN	WALL pull out wakeup enable in S2 mode	RW	0

		0:disable 1:enable When this bit is enabled, if WALL if pulled out, working mode will be switched from S2 to S1. The wakup voltage of pull out operation is PMU_SYS_CTL0[2:1]		
1	USB_S2WK_FLAG	VBUS pull out wakeup flag in S2 mode 1:VBUS pull out wakeup in S2 0:No VBUS pull out wakeup in S2	R	0
0	WALL_S2WK_FLAG	WALL pull out wakeup flag in S2 mode 1:WALL pull out wakeup in S2 0:No WALL pull out wakeup in S2	R	0

7.4.5 PMU_SYS_CTL4

PMU_SYS_CTL4 Register (RTCVDD) (default 0x0080)
Offset = 0x04

Bit(s)	Name	Description	Access	Reset
15:0	-	Reserved	-	-

7.4.6 PMU_SYS_CTL5

PMU_SYS_CTL5 Register (RTCVDD) (default 0x0180)
Offset = 0x05

Bit(s)	Name	Description	Access	Reset
15	OVSD_EN	Overvoltage turnoff enable bit 0: 7V hardware turn off enable 1: 7V hardware turn off disable *Note: Only for CHIP_VER(0xDC)=0x1)*	RW	0
14:11	-	Reserved	-	-
10	ONOFF_8S_SEL	ONOFF long press for 8sec restart selection 0: reset after long press, then restart 1: reset after long press, then shut down and enter S4	RW	0
9	REMCON_DECT_EN	REMCON wakeup detection enable 0: Disable 1: Enable	RW	0
8	VBUSWKDTEN	VBUS wakeup detect enable 0: Disable 1: Enable	RW	1
7	WALLWKDTEN	WALL wakeup detect enable	RW	1

		0: Disable 1: Enable		
6:5	IBIAS	IBIAS 00:lower 01:low 10:high 11:higher	RW	0x0
4:0	-	Reserved	-	-

7.4.7 PMU_BAT_CTL0

PMU_BAT_CTL0 Register (RTCVDD) (default 0x5680)
Offset = 0x0A

Bit(s)	Name	Description	Access	Reset
15:14	BAT_UV_VOL	BAT Undervoltage interrupt voltage setting 00:3.1V 01:3.3V 10:3.4V 11:3.5V	RW	01
13:12	BAT_OV_VOL	BAT overvoltage interrupt voltage setting 00:4.3V 01:4.4V 10:4.5V 11:4.8V	RW	01
11:8	BAT_OC_SET	BAT overcurrent interrupt current setting 0000:200mA 0001:250mA 0010:300mA 0011:350mA 0100:400mA 0101:450mA 0110:500mA 0111:550mA 1000:600mA 1001:650mA 1010:700mA 1011:750mA 1100:800mA 1101:850mA 1110:900mA 1111:950mA The current detected is flowing from BAT to SYSPWR through the diode, overcurrent signal	RW	0110

		debounce time is 1ms.		
7:6	BAT_OC_SHUTOFF_SET	BAT overcurrent shutoff current setting 00:600mA 01:800mA 10:1000mA 11:1200mA Overcurrent signal debounce is 1ms	RW	10
5:0	-	Reserved	-	-

7.4.8 PMU_BAT_CTL1

PMU_BAT_CTL1 Register (RTCVDD) (default 0xFC00)
Offset = 0x0B

Bit(s)	Name	Description	Access	Reset
15	BAT_OC_EN	BAT overcurrent detection enable 0:disable 1:enable	RW	1
14	BAT_OV_EN	BAT overvoltage detection enable 0:disable 1:enable	RW	1
13	BAT_UV_EN	BAT undervoltage detection enable 0:disable 1:enable	RW	1
12	BAT_OC_INT_EN	BAT overcurrent interrupt enable 0:disable 1:enable	RW	1
11	BAT_OV_INT_EN	BAT overvoltage interrupt enable 0:disable 1:enable	RW	1
10	BAT_UV_INT_EN	BAT undervoltage interrupt enable 0:disable 1:enable	RW	1
9	BAT_OC_SHUTOFF_EN	BAT overcurrent cutoff enable 0:disable 1:enable	RW	0
8:0	-	Reserved	-	-

7.4.9 PMU_VBUS_CTL0

PMU_VBUS_CTL0 Register (RTCVDD) (default 0xA680)
Offset = 0x0C

Bit(s)	Name	Description	Access	Reset

15:14	VBUS_UV_VOL	VBUS undervoltage interrupt voltage setting 00:3.8V 01:4.0V 10:4.3V 11:4.5V	RW	10
13:12	VBUS_OV_VOL	VBUS overvoltage interrupt voltage setting *For CHIP_VER(0xDC)=0x0:* 00:5.3V 01:5.5V 10:5.6V 11:5.8V *For CHIP_VER(0xDC)=0x1:* 00:5.5V 01:5.8V 10:6.3V 11:6.8V	RW	0x2
11:8	VBUS_OC_SET	VBUS overcurrent interrupt current setting 0000:100mA 0001:500mA 0010:600mA 0011:700mA 0100:800mA 0101:900mA 0110:1000mA Others: reserved The current under detection is the current flowing from VBUS to SYSPWR through the diode, the overcurrent signal debounce time is 1ms	RW	0110
7:6	VBUS_OC_SHUTOFF_SET	VBUS overcurrent shutoff current setting 00:600mA 01:800mA 10:1000mA 11:1200mA The overcurrent signal debounce time is 1ms	RW	10
5:0	-	Reserved	-	-

7.4.10 PMU_VBUS_CTL1

PMU_VBUS_CTL1 Register (RTCVDD) (default 0xFC00)
Offset = 0x0D

Bit(s)	Name	Description	Access	Reset
15	VBUS_OC_EN	VBUS overcurrent detection enable 0:disable 1:enable	RW	1
14	VBUS_OV_EN	VBUS overvoltage detection enable 0:disable 1:enable	RW	1
13	VBUS_UV_EN	VBUS undervoltage detection enable 0:disable 1:enable	RW	1
12	VBUS_OC_INT_EN	VBUS overcurrent interrupt enable 0:disable 1:enable	RW	0
11	VBUS_OV_INT_EN	VBUS overvoltage interrupt enable 0:disable 1:enable	RW	0
10	VBUS_UV_INT_EN	VBUS undervoltage interrupt enable 0:disable 1:enable	RW	0
9	VBUS_OC_SHUTOFF_EN	VBUS overcurrent shutoff enable 0:disable 1:enable	RW	0
8	VBUS_DETECT_INT_EN	VBUS plug in/pull out interrupt enable 0:disable 1:enable The relative interrupt voltage is decided by PMU_SYS_PENDING[6:5]	RW	0
7:0	-	Reserved	-	-

7.4.11 PMU_WALL_CTL0

PMU_WALL_CTL0 Register (RTCVDD) (default 0xE680)
Offset = 0x0E

Bit(s)	Name	Description	Access	Reset
15:14	WALL_UV_VOL	WALL undervoltage interrupt voltage setting 00:3.8V 01:4.0V 10:4.3V	RW	0x3

		11:4.5V		
13:12	WALL_OV_VOL	WALL overvoltage interrupt voltage setting *For CHIP_VER(0xDC)=0x0:00:5.3V* 01:5.5V 10:5.6V 11:5.8V *For CHIP_VER(0xDC)=0x1:* 00:5.5V 01:5.8V 10:6.3V 11:6.8V	RW	0x2
11:8	WALL_OC_SET	WALL overcurrent interrupt current setting 0000:200mA 0001:250mA 0010:300mA 0011:350mA 0100:400mA 0101:450mA 0110:500mA 0111:550mA 1000:600mA 1001:650mA 1010:700mA 1011:750mA 1100:800mA 1101:850mA 1110:900mA 1111:950mA The current under detection is flowing from WALL to SYSPWR, through the diode, the overcurrent signal debounce time is 1ms	RW	0x6
7:6	WALL_OC_SHUTOFF_SET	WALL overcurrent shutoff current setting 00:600mA 01:800mA 10:1000mA 11:1200mA Overcurrent signal debounce time is 1ms	RW	0x2
5:0	-	Reserved	-	-

7.4.12 PMU_WALL_CTL1

PMU_WALL_CTL1 Register (RTCVDD) (default 0xFC00)
Offset = 0x0F

Bit(s)	Name	Description	Access	Reset
15	WALL_OC_EN	WALL overcurrent detection enable 0:disable 1:enable	RW	1
14	WALL_OV_EN	WALL overvoltage detection enable 0:disable 1:enable	RW	1
13	WALL_UV_EN	WALL undervoltage detection enable 0:disable 1:enable	RW	1
12	WALL_OC_INT_EN	WALL overcurrent interrupt enable 0:disable 1:enable	RW	1
11	WALL_OV_INT_EN	WALL overvoltage interrupt enable 0:disable 1:enable	RW	1
10	WALL_UV_INT_EN	WALL undervoltage interrupt enable 0:disable 1:enable	RW	1
9	WALL_OC_SHUTOFF_EN	WALL overcurrent shutoff enable 0:disable 1:enable	RW	0
8	WALL_DETECT_INT_EN	WALL plug in/pull out interrupt enable 0:disable 1:enable The interrupt voltage is decided by PMU_SYS_PENDING[4:3]	RW	0
7:0	-	Reserved	-	-

7.4.13 PMU_SYS_PENDING

PMU_SYS_PENDING Register (RTCVDD) (default 0x0000)
Offset = 0x10

Bit(s)	Name	Description	Access	Reset
15	BAT_OV_STATUS	BAT overvoltage flag 0:BAT is not overvoltage 1:BAT is overvoltage	R	0x0
14	BAT_UV_STATUS	BAT undervoltage state flag 0:BAT is not undervoltage 1:BAT is undervoltage	R	0x0
13	BAT_OC_STATUS	BAT overcurrent state flag 0:BAT is not overcurrent 1:BAT is overcurrent	R	0x0

12	VBUS_OV_STATUS	VBUS overvoltage state flag 0:BAT is not overvoltage 1:BAT is overvoltage	R	0x0
11	VBUS_UV_STATUS	VBUS undervoltage state flag 0:BAT is not undervoltage 1:BAT is undervoltage	R	0x0
10	VBUS_OC_STATUS	VBUS overcurrent state flag 0:BAT is not overcurrent 1:BAT is overcurrent	R	0x0
9	WALL_OV_STATUS	WALL overvoltage state flag 0:BAT is not overvoltage 1:BAT is overvoltage	R	0x0
8	WALL_UV_STATUS	WALL undervoltage state flag 0:BAT is not undervoltage 1:BAT is undervoltage	R	0x0
7	WALL_OC_STATUS	WALL overcurrent state flag 0:BAT is not overcurrent 1:BAT is overcurrent	R	0x0
6	VBUS_IN_PD	VBUS plug in (VBUS ADC voltage higher than 3.2V) pending 0:VBUS is not plugged in 1: VBUS is plugged in	R	0x0
5	VBUS_OUT_PD	VBUS pull out (VBUS ADC voltage lower than 3.0V) pending 0:VBUS is not pulled out 1: VBUS is pulled out	R	0x0
4	WALL_IN_PD	WALL is plugged in (WALL ADC voltage higher than 3.2V) pending 0:WALL is not plugged in 1: WALL is plugged in	R	0x0
3	WALL_OUT_PD	WALL pull out (WALL ADC voltage lower than 3.0V) pending 0:WALL is not pulled out 1: VBUS is pulled out	R	0x0
2:1	-	Reserved	-	-
0	STATUS_CLEAR1	Status flag clear bit Writing 1 to this bit will clear PMU_SYS_PENDING[15:3], then this bit will turn to 0 automatically	RW	0x0

7.4.14 PMU_DC1_CTL0

PMU_DC1_CTL0 Register (RTCVDD) (default 0x8628)

Offset = 0x11

Bit(s)	Name	Description	Access	Reset
15:13	FSL	DC-DC OSC frequency setting 000~011: slower 100:1.60MHz 101~111: higher	RW	0x4
12	-	Reserved	-	-
11:7	DC1_VOL	DC-DC1(VDD) Voltage setting 00000:0.700V 00001:0.725V …… 01100:1.00V …… 11100:1.40V Others:reserved DC-DC1_VOLTAGE = 0.7V+ DC-DC1_VOL*25mV	RW	0xc
6	DC1_MOD	DC1 modulation mode 0: PFM mode 1: PWM mode	RW	0
5	DC1_MODEN1L	DC-DC1 automatic mode switching enable 0:Disable 1:Enable When this bit is 0, DC-DC1 mode is decided by bit[6]	RW	1
4	DC1_AT_CURL	DC-DC1 mode switch from PWM to PFM, peak conductance current threshold setting 0:smaller 1:bigger	RW	0
3	DC1_EN_CSL	DC-DC1 conductance current detection circuit enable 0:Disable 1:Enable	RW	1
2:1	DC1_CS_RL	DC-DC2 conductor current detecting circuit setting 00:small 01:1.30A 10:medium 11:High	RW	0
0	DC1_PFMOCP_THL	DC-DC1 PFM mode current limit selection 0:smaller 1:bigger	RW	0

7.4.15 PMU_DC2_CTL0

PMU_DC2_CTL0 Register (RTCVDD) (default 0x088A)
Offset = 0x14

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th><th>Access</th><th>Reset</th></tr>
<tr><td>15</td><td>DC2_EN</td><td>DC-DC2 enable
0: disable
1: enable</td><td>RW</td><td>0</td></tr>
<tr><td>14:13</td><td>-</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>12:8</td><td>DC2_VOL</td><td>DCDC2 (VDDR) Voltage setting
<table>
<tr><td>CHIP_VER(0xDC)
=0x1:</td><td>CHIP_VER(0xDC)
=0x0:</td></tr>
<tr><td>00000:1.00V</td><td>00000:1.30V</td></tr>
<tr><td>00001:1.05V</td><td>00001:1.35V</td></tr>
<tr><td>00010:1.10V</td><td>00010:1.40V</td></tr>
<tr><td>00011:1.15V</td><td>00011:1.45V</td></tr>
<tr><td>00100:1.20V</td><td>00100:1.50V</td></tr>
<tr><td>00101:1.25V</td><td>00101:1.55V</td></tr>
<tr><td>00110:1.30V</td><td>00110:1.60V</td></tr>
<tr><td>00111:1.35V</td><td>00111:1.65V</td></tr>
<tr><td>01000:1.40V</td><td>01000:1.70V</td></tr>
<tr><td>01001:1.45V</td><td>01001:1.75V</td></tr>
<tr><td>01010:1.50V</td><td>01010:1.80V</td></tr>
<tr><td>01011:1.55V</td><td>01011:1.85V</td></tr>
<tr><td>01100:1.60V</td><td>01100:1.90V</td></tr>
<tr><td>01101:1.65V</td><td>01101:1.95V</td></tr>
<tr><td>01110:1.70V</td><td>01110:2.05V</td></tr>
<tr><td>01111:1.75V</td><td>01111:2.15V</td></tr>
<tr><td>10000:1.80V</td><td>10000:reseved</td></tr>
<tr><td>10001:1.85V</td><td>10001:reseved</td></tr>
<tr><td>Others:1.85v</td><td>Others:reseved</td></tr>
</table></td><td>RW</td><td>0x8</td></tr>
<tr><td>7</td><td>DC2_LOOP_EN</td><td>DC2 phase margin improve enable:
0: disable
1: enable
Note: only for CHIP_VER(0xC)=0x1</td><td>RW</td><td>1</td></tr>
<tr><td>6</td><td>DC2_MOD</td><td>DC-DC2 modulation mode
0: PFM mode
1: PWM mode</td><td>RW</td><td>0</td></tr>
<tr><td>5</td><td>DC2_MODEN1
L</td><td>DC-DC2 auto mode switching circuit enable
0:Disable
1:Enable
When this bit is 0, DC-DC2 mode is determined by bit[6]</td><td>RW</td><td>0</td></tr>
</table>

4	DC2_AT_CURL	DC-DC2 PWM mode switch to PFM mode conductor peak current threshold setting 0 :Smaller 1 :bigger	RW	0
3	DC2_EN_CSL	DC-DC2 conductor current detecting circuit enable 0:Disable 1:Enable	RW	1
2:1	DC2_CS_RL	DC-DC2 conductor current detecting circuit setting 00:small 01:1.25A 10:medium 11:High	RW	1
0	DC2_PFMOCP_THL	DC-DC2 PFM mode current limiting value selection 0 :Smaller 1 :Bigger	RW	0

7.4.16 PMU_DC3_CTL0

PMU_DC3_CTL0 Register (RTCVDD) (default 0x8B8A)
Offset = 0x17

Bit(s)	Name	Description	Access	Reset
15:11	-	Reserved	-	-
12	DC3_PD	DC-DC3 output pull-down resister 1: enable pull-down resister 0: disable pull-down resister Note: only for CHIP_VER(0xC)=0x1	RW	0
11:9	DC3_VOL	DC-DC3(VCC) Voltage setting 000:2.6V 001:2.7V 010:2.8V 011:2.9V 100:3.0V 101:3.1V 110:3.2V 111:3.3V	RW	0x5
8	EN_SETVCCL	Working circuit selection 0: according to bit[7] 1: LDO mode	RW	1
7	SETVCCL	DC3VOUT working circuit selection 0:LDO mode 1:DC-DC mode	RW	1
6	DC3_MOD	DC-DC3 modulation mode	RW	0

		0: PFM mode 1: PWM mode		
5	DC3_MODEN1L	DC-DC3 auto mode switch circuit enable 0:Disable 1:Enable When this bit is 0, DC-DC3 mode is decided by bit[6]	RW	0
4	DC3_AT_CURL	DC-DC3 mode switch to PFM mode conductor peak current threshold setting 0 :Smaller 1 :Bigger	RW	0
3	DC3_EN_CSL	DC-DC3 conductor current detection circuit enable 0:Disable 1:Enable	RW	1
2:1	DC3_CS_RL	DC-DC3 conductor current detecting circuit setting 00:small 01:1.33A 10:medium 11:High	RW	1
0	DC3_PFMOCP_THL	DC3PFM mode current limit value selection 0 :Smaller 1 :Bigger	RW	0

7.4.17 PMU_LDO1_CTL

PMU_LDO1_CTL Register (RTCVDD) (default 0xA000)
Offset = 0x1E

Bit(s)	Name	Description	Access	Reset
15:13	LDO1_VOL	LDO1(AVCC1) Voltage setting 000:2.6V 001:2.7V 010:2.8V 011:2.9V 100:3.0V 101:3.1V 110:3.2V 111:3.3V	RW	0x5
12	LDO1_SOFT_STARTUP	Soft startup select 0: fast power on 1: slow power on	RW	0
11	LDO1_BIAS	Bias select	RW	0

		0: small bias current 1: big bias current		
10:0	-	Reserved	-	-

7.4.18 PMU_LDO2_CTL

PMU_LDO2_CTL Register (RTCVDD) (default 0xA000)
Offset = 0x1F

Bit(s)	Name	Description	Access	Reset
15:13	LDO2_VOL	LDO2(AVCC2) Voltage setting 000:2.6V 001:2.7V 010:2.8V 011:2.9V 100:3.0V 101:3.1V 110:3.2V 111:3.3V	RW	0x5
12	LDO2_SOFT_STARTUP	Soft startup select 0: fast power on 1: slow power on	RW	0
11	LDO2_BIAS	Bias select 0: small bias current 1: big bias current	RW	0
10:0	-	Reserved	-	-

7.4.19 PMU_LDO3_CTL

PMU_LDO3_CTL Register (RTCVDD) (default 0x6000)
Offset = 0x20

Bit(s)	Name	Description	Access	Reset
15:13	LDO3_VOL	LDO3(VDD_18) Voltage setting 000:1.5V 001:1.6V 010:1.7V 011:1.8V 100:1.9V 101:2.0V Others:Reserved	RW	0x3
12	LDO3_SOFT_STARTUP	Soft startup select 0: fast power on 1: slow power on	RW	0

11	LDO3_BIAS	Bias select 0: small bias current 1: big bias current	RW	0
10:0	-	Reserved	-	-

7.4.20 PMU_LDO5_CTL

PMU_LDO5_CTL Register (RTCVDD) (default 0x4000)
Offset = 0x22

Bit(s)	Name	Description	Access	Reset
15:13	LDO5_VOL	LDO5 Voltage setting 000:2.6V 001:2.7V 010:2.8V 011:2.9V 100:3.0V 101:3.1V 110:3.2V 111:3.3V	RW	0x2
12	LDO5_SOFT_STARTUP	Soft startup select 0: fast power on 1: slow power on	RW	0
11	LDO5_BIAS	Bias select 0: small bias current 1: big bias current	RW	0
10:1	-	Reserved	-	-
0	LDO5_EN	LDO5 enable bit 0:disable 1:enable	RW	0

7.4.21 PMU_LDO6_CTL

PMU_LDO6_CTL Register (RTCVDD) (default 0xA000)
Offset = 0x23

Bit(s)	Name	Description	Access	Reset
15:11	LDO6_VOL	LDO6(AVDD1.2) Voltage setting 00000:0.700V 00001:0.725V …… 01100:1.00V …… 10100:1.2V	RW	0x14

		11100:1.40V Others:1.40V LDO6_VOLTAGE = 0.7V+ LDO6_VOL * 25mV		
10	LDO6_SOFT_STARTUP	Soft startup select 0: fast power on 1: slow power on	RW	0
9	LDO6_BIAS	Bias select 0: small bias current 1: big bias current	RW	0
8:0	-	Reserved	-	-

7.4.22 PMU_LDO7_CTL

PMU_LDO7_CTL Register (RTCVDD) (default 0x6000)
Offset = 0x24

Bit(s)	Name	Description	Access	Reset
15:13	LDO7_VOL	LDO7(Analog1.8) Voltage setting 000:1.5V 001:1.6V 010:1.7V 011:1.8V 100:1.9V 101:2.0V Others:2.0V	RW	0x3
12	LDO7_SOFT_STARTUP	Soft startup select 0: fast power on 1: slow power on	RW	0
11	LDO7_bias	Bias select 0: small bias current 1: big bias current	RW	0
10:1	-	Reserved	-	-
0	LDO7_EN	LDO7 enable bit 0:disable 1:enable	RW	0

7.4.23 PMU_LDO11_CTL

PMU_LDO12_CTL Register (RTCVDD) (default 0xB000)
Offset = 0x28

Bit(s)	Name	Description	Access	Reset
15:13	LDO11_VOL	LDO11(SVCC) Voltage setting	RW	0x5

		000:2.6V 001:2.7V 010:2.8V 011:2.9V 100:3.0V 101:3.1V 110:3.2V 111:3.3V		
12	SVCC_LOW_EN	SVCC low voltage protection enable (Analog use only) 0:Disable 1:Enable	RW	1
11:0	-	Reserved	-	-

7.4.24 PMU_SWITCH_CTL

PMU_SWITCH_CTL Register (RTCVDD) (default 0x0000)
Offset = 0x29

Bit(s)	Name	Description	Access	Reset
15	SWITCH1_EN	SWITCH1_EN 0:enable 1:disable	RW	0
14:6	-	Reserved	-	-
5	SWITCH1_MODE	SWITCH1 mode selection 0:LDO 1:SWITCH	RW	0
4:3	SWITCH1_LDO_VOL	Voltage setting when SWITCH1 used as LDO 00:3.0V 01:3.1V 10:3.2V 11:3.3V	RW	0
2	-	Reserved	-	-
1	SWITCH1_DISCHARGE_EN	SWITCH1 discharging enable control 0:Disable 1:Enable Bit[1] and bit[2] cannot be 1 at the same time; bit[1] and bit[15] cannot be 1 at the same time	RW	0
0	SWITCH1_LDO_BIAS	BIAS current select: 0: small bias current 1: big bias current	RW	0

7.4.25 PMU_OV_CTL0

PMU_OV_CTL0 Register (RTCVDD) (default 0x5555)
Offset = 0x2A

Bit(s)	Name	Description	Access	Reset
15	-	Reserved	-	-
14	DC-DC1_OV_SET	DC-DC1 output overvoltage setting 0:+10% DC1OUT 1:+20% DC1OUT If DC1OUT is detected higher than settings for 1ms, and the relative enable bit is 1, DC-DC1 overvoltage interrupt will be sent out	RW	1
13	-	Reserved	-	-
12	DC-DC2_OV_SET	DC-DC2 output overvoltage setting 0:+10% DC2OUT 1:+20% DC2OUT If DC2OUT is detected higher than settings for 1ms, and the relative enable bit is 1, DC-DC2 overvoltage interrupt will be sent out	RW	1
11	-	Reserved	-	-
10	DC-DC3_OV_SET	DC-DC3 output overvoltage setting 0:+10% DC3OUT 1:+20% DC3OUT If DC3OUT is detected higher than settings for 1ms, and the relative enable bit is 1, DC-DC3 overvoltage interrupt will be sent out	RW	1
9:8	-	Reserved	-	-
7:6	LDO1_OV_SET	LDO1 output overvoltage setting 00:+7% LDO1OUT 01:+11% LDO1OUT 10:+15% LDO1OUT 11:+20% LDO1OUT If LDO1OUT is detected higher than settings for 1ms, and the relative enable bit is 1, LDO1 overvoltage interrupt will be sent out	RW	1
5:4	LDO2_OV_SET	LDO2 output overvoltage setting 00:+5% LDO2OUT 01:+10% LDO2OUT 10:+15% LDO2OUT 11:+20% LDO2OUT	RW	1

		If LDO2OUT is detected higher than settings for 1ms, and the relative enable bit is 1, LDO2 overvoltage interrupt will be sent out		
3:2	LDO3_OV_SET	LDO3 output overvoltage setting 00:5% LDO3OUT 01:10% LDO3OUT 10:15% LDO3OUT 11:20% LDO3OUT If LDO3OUT is detected higher than settings for 1ms, and the relative enable bit is 1, LDO3 overvoltage interrupt will be sent out	RW	1
1:0	-	Reserved	-	-

7.4.26 PMU_OV_CTL1

PMU_OV_CTL1 Register (RTCVDD) (default 0x5550)
Offset = 0x2B

Bit(s)	Name	Description	Access	Reset
15:14	LDO5_OV_SET	LDO5 output overvoltage voltage setting 00:5% LDO5OUT 01:10% LDO5OUT 10:15% LDO5OUT 11:20% LDO5OUT If LDO5OUT voltage is higher than its settings for 1ms, and the relative enable bit is 1, LDO5 overvoltage interrupt will be sent.	RW	1
13:12	LDO6_OV_SET	LDO6 output overvoltage voltage setting 00:5% LDO6OUT 01:10% LDO6OUT 10:15% LDO6OUT 11:20% LDO6OUT If LDO6OUT voltage is higher than its settings for 1ms, and the relative enable bit is 1, LDO6 overvoltage interrupt will be sent.	RW	1
11:10	LDO7_OV_SET	LDO7 output overvoltage voltage setting 00:5% LDO7OUT 01:10% LDO7OUT 10:15% LDO7OUT 11:20% LDO7OUT If LDO7OUT voltage is higher than its settings for 1ms, and the relative enable bit is 1, LDO7	RW	1

		overvoltage interrupt will be sent.		
9:0	-	Reserved	-	-

7.4.27 PMU_OV_STATUS

PMU_OV_STATUS Register (RTCVDD) (default 0x0000)
Offset = 0x2C

Bit(s)	Name	Description	Access	Reset
15	DC-DC1_OV_STATUS	DC-DC1 output overvoltage flag 0: DC-DC1 is not overvoltage at present 1: DC-DC1 is overvoltage at present	R	0
14	DC-DC2_OV_STATUS	DC-DC2 output overvoltage flag 0: DC-DC2 is not overvoltage at present 1: DC-DC2 is overvoltage at present	R	0
13	DC-DC3_OV_STATUS	DC-DC3 output overvoltage flag 0: DC-DC3 is not overvoltage at present 1: DC-DC3 is overvoltage at present	R	0
12	-	Reserved	-	-
11	LDO1_OV_STATUS	LDO1 output overvoltage flag 0: LDO1 not overvoltage at present 1: LDO1 is overvoltage at present	R	0
10	LDO2_OV_STATUS	LDO2 output overvoltage flag 0: LDO2 not overvoltage at present 1: LDO2 is overvoltage at present	R	0
9	LDO3_OV_STATUS	LDO3 output overvoltage flag 0: LDO3 not overvoltage at present 1: LDO3 is overvoltage at present	R	0
8	-	Reserved	-	-
7	LDO5_OV_STATUS	LDO5 output overvoltage flag 0: LDO5 not overvoltage at present 1: LDO5 is overvoltage at present	R	0
6	LDO6_OV_STATUS	LDO6 output overvoltage flag 0: LDO6 not overvoltage at present 1: LDO6 is overvoltage at present	R	0
5	LDO7_OV_STATUS	LDO7 output overvoltage flag 0: LDO7 not overvoltage at present 1: LDO7 is overvoltage at present	R	0
4:1	-	Reserved	-	-
0	STATUS_CLEAR2	Flag clear bit: When writing 1 to this bit will clear bit[15:4], then this bit turn to 0 automatically	RW	0

7.4.28 PMU_OV_EN

PMU_OV_EN Register (RTCVDD) (default 0xFFFC)
Offset = 0x2D

Bit(s)	Name	Description	Access	Reset
15	DC-DC1_OV_EN	DC-DC1 output overvoltage detection enable 0:Disable 1:Enable	RW	1
14	DC-DC2_OV_EN	DC-DC2 output overvoltage detection enable 0:Disable 1:Enable	RW	1
13	DC-DC3_OV_EN	DC-DC3 output overvoltage detection enable 0:Disable 1:Enable	RW	1
12	-	Reserved	-	-
11	LDO1_OV_EN	LDO1 output overvoltage detection enable 0:Disable 1:Enable	RW	1
10	LDO2_OV_EN	LDO2 output overvoltage detection enable 0:Disable 1:Enable	RW	1
9	LDO3_OV_EN	LDO3 output overvoltage detection enable 0:Disable 1:Enable	RW	1
8	-	Reserved	-	-
7	LDO5_OV_EN	LDO5 output overvoltage detection enable 0:Disable 1:Enable	RW	1
6	LDO6_OV_EN	LDO6 output overvoltage detection enable 0:Disable 1:Enable	RW	1
5	LDO7_OV_EN	LDO7 output overvoltage detection enable 0:Disable 1:Enable	RW	1
4:0	-	Reserved	-	-

7.4.29 PMU_OV_INT_EN

PMU_OV_INT_EN Register (RTCVDD) (default 0xFFFC)
Offset = 0x2E

Bit(s)	Name	Description	Access	Reset
15	DC-DC1_OV_INT_E	DC-DC1 output overvoltage interrupt	RW	1

	N	enable 0:Disable 1:Enable		
14	DC-DC2_OV_INT_EN	DC-DC2 output overvoltage interrupt enable 0:Disable 1:Enable	RW	1
13	DC-DC3_OV_INT_EN	DC-DC3 output overvoltage interrupt enable 0:Disable 1:Enable	RW	1
12	-	Reserved	-	-
11	LDO1_OV_INT_EN	LDO1 output overvoltage interrupt enable 0:Disable 1:Enable	RW	1
10	LDO2_OV_INT_EN	LDO2 output overvoltage interrupt enable 0:Disable 1:Enable	RW	1
9	LDO3_OV_INT_EN	LDO3 output overvoltage interrupt enable 0:Disable 1:Enable	RW	1
8	-	Reserved	-	-
7	LDO5_OV_INT_EN	LDO5 output overvoltage interrupt enable 0:Disable 1:Enable	RW	1
6	LDO6_O_INT V_EN	LDO6 output overvoltage interrupt enable 0:Disable 1:Enable	RW	1
5	LDO7_OV_INT_EN	LDO7 output overvoltage interrupt enable 0:Disable 1:Enable	RW	1
4:0	-	Reserved	-	-

7.4.30 PMU_OC_CTL

PMU_OV_CTL Register (RTCVDD) (default 0x0000)
Offset = 0x2F

Bit(s)	Name	Description	Access	Reset
15	LDO1_OC_SET	LDO1 output overcurrent current setting 0:800mA 1:900mA If LDO1 is overcurrent, it will enter standby mode.	RW	0

14	LDO2_OC_SET	LDO2 output overcurrent current setting 0:400mA 1:500mA If LDO2 is overcurrent, it will enter standby mode.	RW	0
13	LDO3_OC_SET	LDO3 output overcurrent current setting 0:500mA 1:600mA If LDO3 is overcurrent, it will enter standby mode.	RW	0
12	-	Reserved	-	-
11	LDO5_OC_SET	LDO5 output overcurrent current setting 0:300mA 1:400mA If LDO5OUT output current exceeds the settings, and the relative interrupt is enabled, then overcurrent interrupt will be sent and LDO5 will be shut down. When the software responds the interrupt, its interrupt flag bit should be cleared to 0. Disable then enable the LDO, the LDO will be turned on, **or** disable the overcurrent detection enable bit, then turn on the LDO.	RW	0
10	LDO6_OC_SET	LDO6 output overcurrent current setting 0:400mA 1:500Ma If LDO6 is overcurrent, it will enter standby mode.	RW	0
9	LDO7_OC_SET	LDO7 output overcurrent current setting 0:400mA 1:500mA If LDO7OUT output current exceeds the settings, and the relative interrupt is enabled, then overcurrent interrupt will be sent and LDO7 will be shut down. When the software responds the interrupt, its interrupt flag bit should be cleared to 0. Disable then enable the LDO, the LDO will be turned on, **or** disable the overcurrent detection enable bit, then turn on the LDO.	RW	0
8:0	-	Reserved	-	-

7.4.31 PMU_OC_STATUS

PMU_OC_STATUS Register (RTCVDD) (default 0x0000)
Offset = 0x30

Bit(s)	Name	Description	Access	Reset
15	LDO1_OC_STATUS	LDO1 output overcurrent flag 0:LDO1 is not overcurrent at present 1:LDO1 is overcurrent at present When LDO is overcurrent, this bit will be 1, and the LDO will be shutdown by HW	R	0
14	LDO2_OC_STATUS	LDO2 output overcurrent current flag 0:LDO2 is not overcurrent at present 1:LDO2 is overcurrent at present When LDO is overcurrent, this bit will be 1, and the LDO will be shutdown by HW	R	0
13	LDO3_OC_STATUS	LDO3 output overcurrent current flag 0:LDO3 is not overcurrent at present 1:LDO3 is overcurrent at present When LDO is overcurrent, this bit will be 1, and the LDO will be shutdown by HW	R	0
12	-	Reserved	-	-
11	LDO5_OC_STATUS	LDO5 output overcurrent current flag 0:LDO5 is not overcurrent at present 1:LDO5 is overcurrent at present When LDO is overcurrent, this bit will be 1, and the LDO will be shutdown by HW	R	0
10	LDO6_OC_STATUS	LDO6 output overcurrent current flag 0:LDO6 is not overcurrent at present 1:LDO6 is overcurrent at present When LDO is overcurrent, this bit will be 1, and the LDO will be shutdown by HW	R	0
9	LDO7_OC_STATUS	LDO7 output overcurrent current flag 0:LDO7 is not overcurrent at present 1:LDO7 is overcurrent at present When LDO is overcurrent, this bit will be 1, and the LDO will be shutdown by HW	R	0
8:1	-	Reserved	-	-
0	STATUS_CLEAR3	Flag clear bit: When writing 1 to this bit will clear bit[15:2], then this bit turn to 0 automatically	RW	0

7.4.32 PMU_OC_EN

PMU_OC_EN Register (RTCVDD) (default 0xFFC0)
Offset = 0x31

Bit(s)	Name	Description	Access	Reset
15	LDO1_OC_EN	LDO1 output overcurrent detection enable 0:Disable 1:Enable	RW	1
14	LDO2_OC_EN	LDO2 output overcurrent detection enable 0:Disable 1:Enable	RW	1
13	LDO3_OC_EN	LDO3 output overcurrent detection enable 0:Disable 1:Enable	RW	1
12	Reserved	LDO4 output overcurrent detection enable 0:Disable 1:Enable	RW	1
11	LDO5_OC_EN	LDO5 output overcurrent detection enable 0:Disable 1:Enable	RW	1
10	LDO6_OC_EN	LDO6 output overcurrent detection enable 0:Disable 1:Enable	RW	1
9	LDO7_OC_EN	LDO7 output overcurrent detection enable 0:Disable 1:Enable	RW	1
8:0	-	Reserved	-	-

7.4.33 PMU_OC_INT_EN

PMU_OC_INT_EN Register (RTCVDD) (default 0x1bc0)
Offset = 0x32

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11	LDO5_OC_INT_EN	LDO5 output overcurrent interrupt enable 0:Disable 1:Enable	RW	1
10	-	Reserved	-	-
9	LDO7_OC_INT_EN	LDO7 output overcurrent interrupt enable 0:Disable 1:Enable	RW	1
8:0	-	Reserved	-	-

7.4.34 PMU_UV_CTL0

PMU_UV_CTL0 Register (RTCVDD) (default 0x5555)
Offset = 0x33

Bit(s)	Name	Description	Access	Reset
15	-	Reserved	-	-
14	DC-DC1_UV_SET	DC-DC1 output undervoltage voltage setting 0:10% DC1OUT 1:20% DC1OUT If DC1OUT voltage is lower than setting for 1ms, and the relative enable bit is 1, then DC-DC1 undervoltage interrupt will be sent.	RW	1
13	-	Reserved	-	-
12	DC-DC2_UV_SET	DC-DC2 output undervoltage voltage setting 0:10% DC2OUT 1:20% DC2OUT If DC2OUT voltage is lower than setting for 1ms, and the relative enable bit is 1, then DC-DC2 undervoltage interrupt will be sent.	RW	1
11	-	Reserved	-	-
10	DC-DC3_UV_SET	DC-DC3 output undervoltage voltage setting 0:10% DC3OUT 1:20% DC3OUT If DC3OUT voltage is lower than setting for 1ms, and the relative enable bit is 1, then DC-DC3 undervoltage interrupt will be sent.	RW	1
9:8	-	Reserved	-	-
7:6	LDO1_UV_SET	LDO1 output undervoltage voltage setting 00:5% LDO1OUT 01:10% LDO1OUT 10:15% LDO1OUT 11:20% LDO1OUT If LDO1OUT voltage is lower than setting for 1ms, and the relative enable bit is 1, then LDO1 undervoltage interrupt will be sent.	RW	1
5:4	LDO2_UV_SET	LDO2 output undervoltage voltage setting 00:5% LDO2OUT	RW	1

		01:10% LDO2OUT 10:15% LDO2OUT 11:20% LDO2OUT If LDO2OUT voltage is lower than setting for 1ms, and the relative enable bit is 1, then LDO2 undervoltage interrupt will be sent.		
3:2	LDO3_UV_SET	LDO3 output undervoltage voltage setting 00:5% LDO3OUT 01:10% LDO3OUT 10:15% LDO3OUT 11:20% LDO3OUT If LDO3OUT voltage is lower than setting for 1ms, and the relative enable bit is 1, then LDO3 undervoltage interrupt will be sent.	RW	1
1:0	-	Reserved	-	-

7.4.35 PMU_UV_CTL1

PMU_UV_CTL1 Register (RTCVDD) (default 0x5550)
Offset = 0x34

Bit(s)	Name	Description	Access	Reset
15:14	LDO5_UV_SET	LDO5 output undervoltage voltage setting 00:5% LDO5OUT 01:10% LDO5OUT 10:15% LDO5OUT 11:20% LDO5OUT If LDO5OUT voltage is lower than setting for 1ms, and the relative enable bit is 1, then LDO5 undervoltage interrupt will be sent.	RW	1
13:12	LDO6_UV_SET	LDO6 output undervoltage voltage setting 00:5% LDO6OUT 01:10% LDO6OUT 10:15% LDO6OUT 11:20% LDO6OUT If LDO6OUT voltage is lower than setting for 1ms, and the relative enable bit is 1, then LDO6 undervoltage interrupt will be sent.	RW	1
11:10	LDO7_UV_SET	LDO7 output undervoltage voltage setting 00:5% LDO7OUT 01:10% LDO7OUT 10:15% LDO7OUT	RW	1

		11:20% LDO7OUT If LDO7OUT voltage is lower than setting for 1ms, and the relative enable bit is 1, then LDO7 undervoltage interrupt will be sent.		
9:0	-	Reserved	-	-

7.4.36 PMU_UV_STATUS

PMU_UV_STATUS Register (RTCVDD) (default 0x0000)
Offset = 0x35

Bit(s)	Name	Description	Access	Reset
15	DC-DC1_UV_STATUS	DC-DC1 output undervoltage flag 0:DC-DC1 is not undervoltage at present 1: DC-DC1 is undervoltage at present	R	0
14	DC-DC2_UV_STATUS	DC-DC2 output undervoltage flag 0:DC-DC2 is not undervoltage at present 1: DC-DC2 is undervoltage at present	R	0
13	DC-DC3_UV_STATUS	DC-DC3 output undervoltage flag 0:DC-DC3 is not undervoltage at present 1: DC-DC3 is undervoltage at present	R	0
12	-	Reserved	-	-
11	LDO1_UV_STATUS	LDO1 output undervoltage flag 0:LDO1 is not undervoltage at present 1:LDO1 is undervoltage at present	R	0
10	LDO2_UV_STATUS	LDO2 output undervoltage flag 0:LDO2 is not undervoltage at present 1:LDO2 is undervoltage at present	R	0
9	LDO3_UV_STATUS	LDO3 output undervoltage flag 0:LDO3 is not undervoltage at present 1:LDO3 is undervoltage at present	R	0
8	Reserved	LDO4 output undervoltage flag 0:LDO4 is not undervoltage at present 1:LDO4 is undervoltage at present	R	0
7	LDO5_UV_STATUS	LDO5 output undervoltage flag 0:LDO5 is not undervoltage at present 1:LDO5 is undervoltage at present	R	0
6	LDO6_UV_STATUS	LDO6 output undervoltage flag 0:LDO6 is not undervoltage at present 1:LDO6 is undervoltage at present	R	0
5	LDO7_UV_STATUS	LDO7 output undervoltage flag 0:LDO7 is not undervoltage at present 1:LDO7 is undervoltage at present	R	0
4:1	-	Reserved	-	-

0	Status_Clear4	Flag clear bit: When writing 1 to this bit will clear bit[15:2], then this bit turn to 0 automatically	RW	0

7.4.37 PMU_UV_EN

PMU_UV_EN Register (RTCVDD) (default 0xFFFC)
Offset = 0x36

Bit(s)	Name	Description	Access	Reset
15	DC-DC1_UV_EN	DC-DC1 output undervoltage detection enable 0:Disable 1:Enable	RW	1
14	DC-DC2_UV_EN	DC-DC2 output undervoltage detection enable 0:Disable 1:Enable	RW	1
13	DC-DC3_UV_EN	DC-DC3 output undervoltage detection enable 0:Disable 1:Enable	RW	1
12	-	Reserved	-	-
11	LDO1_UV_EN	LDO1 output undervoltage detection enable 0:Disable 1:Enable	RW	1
10	LDO2_UV_EN	LDO2 output undervoltage detection enable 0:Disable 1:Enable	RW	1
9	LDO3_UV_EN	LDO3 output undervoltage detection enable 0:Disable 1:Enable	RW	1
8	-	Reserved	-	-
7	LDO5_UV_EN	LDO5 output undervoltage detection enable 0:Disable 1:Enable	RW	1
6	LDO6_UV_EN	LDO6 output undervoltage detection enable 0:Disable 1:Enable	RW	1
5	LDO7_UV_EN	LDO7 output undervoltage detection enable 0:Disable 1:Enable	RW	1
4:0	-	Reserved	-	-

7.4.38 PMU_UV_INT_EN

PMU_UV_INT_EN Register (RTCVDD) (default 0xFFFC)
Offset = 0x37

Bit(s)	Name	Description	Access	Reset
15	DC-DC1_UV_INT_EN	DC-DC1 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
14	DC-DC2_UV_INT_EN	DC-DC2 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
13	DC-DC3_UV_INT_EN	DC-DC3 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
12	-	Reserved	-	-
11	LDO1_UV_INT_EN	LDO1 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
10	LDO2_UV_INT_EN	LDO2 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
9	LDO3_UV_INT_EN	LDO3 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
8	-	Reserved	-	-
7	LDO5_UV_INT_EN	LDO5 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
6	LDO6_UV_INT_EN	LDO6 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
5	LDO7_UV_INT_EN	LDO7 output undervoltage interrupt enable 0:Disable 1:Enable	RW	1
4:0	-	Reserved	-	-

7.4.39 PMU_OT_CTL

PMU_OT_CTL Register (RTCVDD) (default 0x3B00)
Offset = 0x38

Bit(s)	Name	Description	Access	Reset
15	OT_STATUS	IC overtemperature flag (limit is	RW	0

		bit[14:13]) 0:not overtemperature at present 1:overtemperature at present Write 1 clear to 0		
14:13	OT_SET	IC overtemperature interrupt temperature setting 00:70°C 01:90°C 10:100°C 11:110°C	RW	1
12	OT_INT_EN	IC overtemperature interrupt enable 0:disable 1:enable	RW	1
11	OT_SHUTOFF_EN	IC overtemperature shut off enable 0:disable 1:enable	RW	1
10:9	OT_SHUTOFF_SET	IC overtemperature temperature setting 00:100°C 01:120°C 10:130°C 11:140°C	RW	1
8	OT_EN	IC overtemperature detection enable 0:disable 1:enable	RW	1
7:0	-	Reserved	-	-

7.4.40 PMU_CHARGER_CTL0

PMU_CHARGER_CTL0 Register (RTCVDD) (default 0x325B)
Offset = 0x39

Bit(s)	Name	Description	Access	Reset
15	ENCH	Enable Charge Circuit 1: Enable charge circuit 0: Disable charge circuit	RW	0
14	CHGTIME	Charger stopping timer set enable bit: 0: disable 1: enable If enable, the charger will stop when the time set by bit[13:12] has arrived.	RW	0
13:12	CHARGE_TIME R1	CC/CV TIMER 00 : 4h 01 : 6h 10 : 8h	RW	0x3

		11 : 12h		
11:10	CHARGE_TIMER2	Trickle timer 00 :30min 01 :40min 10 :50min 11 :60min	RW	0
9	TRICKLEEN	Enable Trickle charge 0: disable 1: enable If this bit is 0, there is no Pre-charging phase, and battery charging goes to Constant current directly.	RW	1
8	CHG_FORCE_OFF	Bit[0] and this bit are enabled at the same time, every bit[7] time the battery voltage will be detected, if the voltage exceeds 4.24V, charging process will be forced to stop 0:Disable 1:Enable	RW	0
7	DTSEL	Charging termination detection time selection 1:once per 20s 0:once per 12min	RW	0
6	CHG_SYSPWR	Set availability of SYSPWR stable loop 0:disable 1:enable When the SYSPWR stable loop is available, charger will control the charging current, ensuring SYSPWR voltage is above its stable value.	RW	1
5:4	CHG_SYSPWR_SET	Set SYSPWR stable value 00:3.81V 01:3.96V 10:4.25V 11:4.40V	RW	1
3	CHG_CURRENT_TEMP	Charging current varies with temperature enable 0:Disable 1:Enable	RW	1
2:1	CHGPWR_SET	Voltage of SYSPWR higher than BAT, then CHPWROK 00:0.1V 01:0.2V 10:0.3V 11:0.4V	RW	1
0	CHGAUTODETE	Auto detection of charging termination	RW	1

	CT_EN	1: enable 0: disable		

Note: When the timer of bit[13:12] or bit[11:10] arrived, bit[8] in PMU_CHARGER_CTL1 register will be set. And when bit[14] is set, charger will be stopped when timer of bit[13:12] arrives.

7.4.41 PMU_CHARGER_CTL1

PMU_CHARGER_CTL1 Register (RTCVDD) (default 0x0040)
Offset = 0x3A

Bit(s)	Name	Description	Access	Reset
15	CHGEND	Charging end Status. 0: not charging over 1: charging over. If battery is not full, this bit is 0; If battery is full, this bit is 1.	R	x
14:13	PHASE	Charging phase 00: Reserved 01: Pre-charging 10: Constant current 11: Constant voltage This two bits will be available only when bit ENCH of this register is set, or will be always read 00	R	x
12	CHGPWROK	CHGPWROK flag 0:SYSPWR voltage is not higher than BAT setting 1:SYSPWR voltage is higher than BAT setting	R	x
11	CUR_ZERO	Charging current is 0 flag 0: Charging current is not 0 1: Charging current is 0	R	x
10	BAT_EXIST	BAT existence flag 0:there is no BAT 1:there is BAT	R	x
9	BAT_DT_OVER	BAT detection finished 1:BAT detection finished 0:BAT detection not finished	R	x
8	CHARGER_TIMER_END	Charger_timer_end flag 0:CC/CV TIMER/ Trickle timer is not finished 1:CC/CV TIMER/ Trickle timer is finished	R	0
7	STOPV	Charger stop voltage (OCV) 0: 4.16V 1: 4.18V In charging, when battery voltage is higher than setting, hardware will stop charging and delay for 1s then detect the battery voltage and every 12 min, if	RW	0

		the voltage is detected higher than setting, then CHGEND bit will be set to 1		
6	CURRENT_SOFT_START	Auto increase/decrease charging current enable 0:Disable 1:Enable When this bit is enabled, charging current is increasing with the time set by bit[8:7]	RW	1
5	BAT_EXIST_EN	Battery detection enable This bit turns from 0 to 1 and delay for 50ms, bit[10] flag is available. If needs to detect again, this bit should be set to 0 then set to 1	RW	0
4	CHARGER_AUTO_CLOSE_EN	When CHGPWROK = 0, whether turn off the charger automatically enable 0:Disable 1:Enable	RW	0
3:0	ICHG_REG_CC	Constant Current charging current configuration 0000:50mA 0001:100mA 0010:200mA 0011:400mA 0100:500mA 0101:600mA 0110:800mA 0111:900mA 1000:1000mA 1001:1200mA 1010:1300mA 1011:1400mA 1100:1600mA 1101:1700mA 1110:1800mA 1111:2000mA	RW	0

7.4.42 PMU_CHARGER_CTL2

PMU_CHARGER_CTL2 Register (RTCVDD) (default 0x0000)
Offset = 0x3B

Bit(s)	Name	Description	Access	Reset
15	-	Reserved	-	-
14:13	TEMPTH1	IC temperature protection threshold1 in charging 00:75°C 01:90°C 10:105°C	RW	0

		11:115°C		
12:11	TEMPTH2	IC temperature protection threshold2 in charging 00:90°C 01:105°C 10:120°C 11:135°C	RW	0
10:9	TEMPTH3	IC temperature protection threshold3 in charging 00:100°C 01:120°C 10:130°C 11:140°C	RW	0
8:7	TIME_STEP	Time Step setting 00:0.5s 01:1s 10:2s 11:4s	RW	0
6	-	Reserved	-	-
5:4	ICHG_REG_T	Charge trickle charging Current Configure 00:50mA 01:100mA 10:200mA 11:300mA	RW	0
3:2	CV_SET	Constant Voltage charging voltage setting 00:4.20V 01:4.30V 10:4.35V 11:4.40V Battery protection board is needed when this bit is not 0. If constant voltage is 4.2V, when the battery voltage is near 4.2V, charging current will decrease gradually, charging time will encrease. To decrease the charging time, set the constant voltage to 4.3V or higher. Note that SYSPWR should be higher than CV_SET.	RW	0
1:0	-	Reserved	-	-

7.4.43 PMU_APDS_CTL

PMU_APDS_CTL0 Register (RTCVDD) (default 0x15F8)
Offset = 0x3D

Bit(s)	Name	Description	Access	Reset
15	VBUS_CONTROL_EN	VBUS voltage current control 0:disable	RW	0

		1:enable When this bit is enabled, the system will adjust the current abstracted from VBUS automatically according to bit[14], ensuring the voltage of VBUS is above the threshold set by bit[11:10] **or** current abstracted from VBUS is smaller than the value set by bit[13:12]. When this bit is disabled, the current will be ensured firstly. If this bit is enabled, bit[8] is invalid.		
14	VBUS_CONTROL_SEL	VBUS control mode selection 0: voltage limiting 1: current limiting	RW	0
13:12	VBUS_CUR_LIMITED	VBUS current limiting threshold 00:1000mA 01:300mA 10:500mA 11:800mA	RW	1
11:10	VBUS_VOL_LIMITED	VBUS voltage limiting threshold 00:4.2V 01:4.3V 10:4.4V 11:4.5V	RW	1
9	VBUS_OTG	USB used as OTG, when VBUS supplies power for external device, VBUS_OTG should be set to 1, preventing VBUS supplies for SYSPWR. 0: enable the diode from VBUS to SYSPWR 1: disable the diode from VBUS to SYSPWR, VBUS and SYSPWR is shut off completely This bit is set to 0 by hardware automatically when entering S2, S3, S4	RW	0
8	VBUS_FST_ON	When SYSPWR is lower than setting, VBUS will be fast on	RW	1
7	VBUS_FST_OFF	When SYSPWR is higher than setting, VBUS will be fast off	RW	1
6	WALL_FST_ON	When SYSPWR is lower than setting, if WALL voltage is enough, WALL will be fast on	RW	1
5	WALL_FST_OFF	When SYSPWR is higher than setting, WALL will be fast off	RW	1

4	BAT_FST_ON	When SYSPWR is lower than setting, if BAT voltage is enough, BAT will be fast on	RW	1
3	BAT_FST_OFF	When SYSPWR is higher than setting, BAT will be fast off	RW	1
2	VBUS_PD	VBUS 5KOhm pull down resistor enable 0: no pull down resistor 1: 5KOhm pull down resistor is pulled down to ground	RW	0
1	WALL_PD	WALL 5KOhm pull down resistor enable 0: no pull down resistor 1: 5KOhm pull down resistor is pulled down to ground	RW	0
0	-	Reserved	-	-

7.4.44 PMU_ICMADC

PMU_ICMADC Register (RTCVDD) (default 0x0000)
Offset = 0x50

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11	CMDATA_OK	0:CMDATA not ready 1:CMDATA ready	R	x
10:0	ICMADC	ICMADC data	R	x

7.4.45 PMU_ABNORMAL_STATUS

PMU_ABNORMAL_STATUS Register (RTCVDD) (default 0x0000)
Offset = 0x62

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9	SVCC_LOW	Quit S1 because of SVCC undervoltage	R	0x0
8	LDO6_OC	Quit S1 because of LDO6 overcurrent	R	0x0
7	LDO3_OC	Quit S1 because of LDO3 overcurrent	R	0x0
6	LDO2_OC	Quit S1 because of LDO2 overcurrent	R	0x0
5	LDO1_OC	Quit S1 because of LDO1 overcurrent	R	0x0
4	VBUS_OC	Quit S1 because of VBUS overcurrent	R	0x0
3	WALL_OC	Quit S1 because of WALL overcurrent	R	0x0
2	BAT_OC	Quit S1 because of BAT overcurrent	R	0x0
1	OT	Quit S1 because of overtemperature	R	0x0
0	BAT_LOW	Quit S1 because of BAT undervoltage	R	0x0

Note: Updating this register when quitting S1

7.4.46 PMU_WALL_APDS_CTL

PMU_WALL_APDS_CTL Register (RTCVDD) (default 0x1400)
Offset = 0x63

Bit(s)	Name	Description	Access	Reset
15	WALL_CONTROL_EN	WALL voltage current control 1: enable 0: disable When this bit is enabled, the system will adjust the current abstracted from WALL automatically according to bit[14], ensuring the voltage of WALL is above the threshold set by bit[11:10] **or** current abstracted from WALL is smaller than the value set by bit[13:12]. When this bit is disabled, the current will be ensured firstly. If this bit is enabled, bit[6] is invalid.	RW	0
14	WALL_CONTROL_SEL	WALL control mode selection 0: voltage limiting 1: current limiting	RW	0
13:12	WALL_CUR_LIMITED	WALL current limiting threshold 00:300mA 01:500mA 10:1500mA 11:2000mA	RW	1
11:10	WALL_VOL_LIMITED	WALL voltage limiting threshold 00:4.2V 01:4.3V 10:4.4V 11:4.5V	RW	1
9	WALL_ID_EN	Diode from WALL to SYSPWR enable 0: enable the diode from WALL to SYSPWR 1: disable the diode from WALL to SYSPWR, VBUS and SYSPWR is shut off completely This bit is set to 0 by hardware automatically when entering S2, S3, S4	RW	0

8:0	-	Reserved	-	-

7.4.47 PMU_REMCON_CTL0

PMU_REMCON_CTL0 Register (RTCVDD) (default 0x0000)
Offset = 0x64

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9	REMCON_WK_4	REMCON voltage range 4 wakeup flag 0:not REMCON voltage range 4 wakeup 1:occur REMCON voltage range 4 wakeup	R	0x0
8	REMCON_WK_3	REMCON voltage range 3 wakeup flag 0:not REMCON voltage range 3 wakeup 1:occur REMCON voltage range 3 wakeup	R	0x0
7	REMCON_WK_2	REMCON voltage range 2 wakeup flag 0:not REMCON voltage range 2 wakeup 1:occur REMCON voltage range 2 wakeup	R	0x0
6	REMCON_WK_1	REMCON voltage range 1 wakeup flag 0:not REMCON voltage range 1 wakeup 1:occur REMCON voltage range 1 wakeup	R	0x0
5	REMCON_WK_0	REMCON voltage range 0 wakeup flag 0:not REMCON voltage range 0 wakeup 1:occur REMCON voltage range 0 wakeup	R	0x0
4	REMCON_WK_EN_4	Enable REMCON voltage range 4 wakeup (2.4V~3.1V) 0:disable 1:enable	RW	0x0
3	REMCON_WK_EN_3	Enable REMCON voltage range 3 wakeup (1.68V~2.4V) 0:disable 1:enable	RW	0x0
2	REMCON_WK_EN_2	Enable REMCON voltage range 2 wakeup (1.03V~1.68V) 0:disable 1:enable	RW	0x0
1	REMCON_WK_EN_1	Enable REMCON voltage range 1 wakeup (0.46V~1.03V) 0:disable 1:enable	RW	0x0
0	REMCON_WK_EN_0	Enable REMCON voltage range 0 wakeup (0V~0.46V) 0:disable 1:enable	RW	0x0

7.4.48 PMU_REMCON_CTL1

PMU_REMCON_CTL1 Register (RTCVDD) (default 0x0000)
Offset = 0x65

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11	REMCON_INT_EN	REMCON interrupt enable 0: Disable 1: Enable	RW	0x0
10	REMCON_PD_CLEAR	Status flag clear bit When writing 1 to this bit, bit[9:5] will be cleared, then this bit turn to 0.	RW	0x0
9	REMCON_PD_4	REMCON voltage range 4 key happen pending 0: REMCON voltage range 4 is not pressed down 1: REMCON voltage range 4 is pressed down Write 1 to clear to 0	RW	0x0
8	REMCON_PD_3	REMCON voltage range 3 key happen pending 0: REMCON voltage range 3 is not pressed down 1: REMCON voltage range 3 is pressed down Write 1 to clear to 0	RW	0x0
7	REMCON_PD_2	REMCON voltage range 2 key happen pending 0: REMCON voltage range 2 is not pressed down 1: REMCON voltage range 2 is pressed down Write 1 to clear to 0	RW	0x0
6	REMCON_PD_1	REMCON voltage range 1 key happen pending 0: REMCON voltage range 1 is not pressed down 1: REMCON voltage range 1 is pressed down Write 1 to clear to 0	RW	0x0
5	REMCON_PD_0	REMCON voltage range 0 key happen pending 0: REMCON voltage range 0 is not pressed down	RW	0x0

		1: REMCON voltage range 0 is pressed down Write 1 to clear to 0		
4	REMCON_INT_EN_4	Enable REMCON voltage range 4 interrupt (2.40V~3.10V) 0: disable 1: enable	RW	0x0
3	REMCON_INT_EN_3	Enable REMCON voltage range 3 interrupt (1.68V~2.40V) 0: disable 1: enable	RW	0x0
2	REMCON_INT_EN_2	Enable REMCON voltage range 2 interrupt (1.03V~1.68V) 0: disable 1: enable	RW	0x0
1	REMCON_INT_EN_1	Enable REMCON voltage range 1 interrupt (0.46V~1.03V) 0: disable 1: enable	RW	0x0
0	REMCON_INT_EN_0	Enable REMCON voltage range 0 interrupt (0V~0.46V) 0: disable 1: enable	RW	0x0

7.4.49 PMU_MUX_CTL0

PMU_MUX_CTL0 Register (RTCVDD) (default 0x0000)
Offset = 0x66

Bit(s)	Name	Description	Access	Reset
15:14	-	Reserved	-	-
13:12	SGPIO5	SGPIO5 Multiplexing 00: SGPIO5(<1MHz) 01: IR 10: Release 32kHz clock 11: Reserved	RW	0
11:10	SGPIO4	SGPIO4 Multiplexing 00: SGPIO4(<1M) 01: IR 10: Release 32kHz clock 11: PWM0	RW	0
9:8	AUXIN2	AUXIN2 Multiplexing 00: AUXIN2 01: SGPIO3(<1MHz)	RW	0

		10: IR 11: Release 32kHz clock		
7:5	AUXIN1	AUXIN0 Multiplexing 000: AUXIN1 001: Reserved 010: IR 011: Release 32kHz clock 100: PWM1 Others: reserved	RW	0
4:2	AUXIN0	AUXIN0 Multiplexing 000: AUXIN0 001: SGPIO1(<1MHz) 010: IR 011: Release 32kHz clock 100: PWM0 Others: reserved	RW	0
1:0	REMCON	REMCON Multiplexing 00: REMCON 01: SGPIO0(<1MHz) 10: IR 11: Release 32kHz clock	RW	0

Note: Release 32 kHz clock is choosed after digital selection.

7.4.50 PMU_SGPIO_CTL0

PMU_SGPIO_CTL0 Register (RTCVDD) (default 0x0000)
Offset = 0x67

Bit(s)	Name	Description	Access	Reset
15	-	Reserved	-	-
14:12	SGPIO[5:3]_PD	SGPIO[5:3]_IRQ pending 0: is not active 1: is active Write 1 to clear to 0	RW	0x0
11	-	Reserved	-	-
10:9	SGPIO[1:0]_PD	SGPIO[1:0]_IRQ pending 0: is not active 1: is active Write 1 to clear to 0	RW	0x0
8	-	Reserved	-	-
7:5	SGPIO[5:3]_INT_EN	SGPIO[5:3] interrupt enable 0: disable 1: enable	RW	0x0
4	-	Reserved	-	-

3:2	SGPIO[1:0]_INT_EN	SGPIO[1:0] interrupt enable 0: disable 1: enable	RW	0x0
1:0	-	Reserved	-	-

7.4.51 PMU_SGPIO_CTL1

PMU_SGPIO_CTL1 Register (RTCVDD) (default 0x0000)
Offset = 0x68

Bit(s)	Name	Description	Access	Reset
15:14	-	Reserved	-	-
13:12	SGPIO5_TPYE	SGPIO5 IRQ type 00:High level active 01:Low level active 10:Rising edge- triggered 11:Falling edge-triggered	RW	0x0
11:10	SGPIO4_TPYE	SGPIO4 IRQ type 00:High level active 01:Low level active 10:Rising edge- triggered 11:Falling edge-triggered	RW	0x0
9:8	SGPIO3_TPYE	SGPIO3IRQ type 00:High level active 01:Low level active 10:Rising edge- triggered 11:Falling edge-triggered	RW	0x0
7:6	-	Reserved	-	-
5:4	SGPIO1_TPYE	SGPIO1IRQ type 00:High level active 01:Low level active 10:Rising edge- triggered 11:Falling edge-triggered	RW	0x0
3:2	SGPIO0_TPYE	SGPIO0 IRQ type 00:High level active 01:Low level active 10:Rising edge-triggered 11:Falling edge-triggered	RW	0x0
1:0	-	Reserved	-	-

7.4.52 PMU_SGPIO_CTL2

PMU_SGPIO_CTL2 Register (RTCVDD) (default 0x0000)

Offset = 0x69

Bit(s)	Name	Description	Access	Reset
15	-	Reserved	-	-
14:12	SGPIO_IRQ_WK_FLAG[5:3]	SGPIO[5:3] IRQ wakeup flag 0: no SGPIO[5:3] wakeup 1: SGPIO0[5:3] wakeup (Quit S1 HW will clear to 0)	R	0x0
11	-	Reserved	-	-
10:9	SGPIO_IRQ_WK_FLAG[1:0]	SGPIO[1:0] IRQ wakeup flag 0: no SGPIO[1:0] wakeup 1: SGPIO0[1:0] wakeup (Quit S1 HW will clear to 0)	R	0x0
8	-	Reserved	-	-
7:5	SGPIO_IRQ_WK_EN[5:3]	SGPIO[5:3]_IRQ wakeup enable 0: disable 1: enable	RW	0x0
4	-	Reserved	-	-
3:2	SGPIO_IRQ_WK_EN[1:0]	SGPIO[1:0]_IRQ wakeup enable 0: disable 1: enable	RW	0x0
1:0	-	Reserved	-	-

7.4.53 PMU_SGPIO_CTL3

PMU_SGPIO_CTL3 Register (RTCVDD) (default 0x0000)

Offset = 0x6A

Bit(s)	Name	Description	Access	Reset
15	-	Reserved	-	-
14:12	SGPIO_OUT_EN[5:3]	SGPIO[5:3] output enable 0:disable 1:enable	RW	0x0
11	-	Reserved	-	-
10:9	SGPIO_OUT_EN[1:0]	SGPIO[1:0] output enable 0:disable 1:enable	RW	0x0
8	-	Reserved	-	-
7:5	SGPIO_IN_EN[5:3]	SGPIO[5:3] input enable 0:disable 1:enable	RW	0x0
4	-	Reserved	-	-
3:2	SGPIO_IN_EN[1:0]	SGPIO[1:0] input enable 0:disable	RW	0x0

		1:enable		
1:0	-	Reserved	-	-

7.4.54 PMU_SGPIO_CTL4

PMU_SGPIO_CTL4 Register (RTCVDD) (default 0x0000)
Offset = 0x6B

Bit(s)	Name	Description	Access	Reset
15:6	-	Reserved	-	-
5:3	SGPIO_DATA[5:3]	SGPIO[5:3] DATA	RW	0x0
2	-	Reserved	-	-
1:0	SGPIO_DATA[1:0]	SGPIO[1:0] DATA	RW	0x0

7.4.55 PWMCLK_CTL

PWM clock controller register (RTCVDD) (default 0x0000)
Offset = 0x6C

Bit(s)	Name	Description	Access	Reset
15:14	-	Reserved	-	-
13	PWM_EN	PWM Module enable 0: disable 1: enable	RW	0x0
12	PWM_RST	PWM Module reset 0: reset 1: normal	RW	0x1
11:10	Q1	Time of Every Duty = 1/32…32/32: Climb up and falling down time: T2 = (Q + 1) * 32 * 32t t is the period of PWMCLKDIV	RW	0x0
9:8	Q0	Time of Every Duty =1/32 …32/32: Climb up and falling down time: T2 = (Q + 1) * 32 * 32t t is the period of PWMCLKDIV	RW	0x0
7:0	PWMCLKDIV	PWM controller clock divisor: 0: /1 1: /2 … 255: /256	RW	0x0

7.4.56 PWM0_CTL

PWM0 control register (RTCVDD) (default 0x0000)
Offset = 0x6D

Bit(s)	Name	Description	Access	Reset
15:8	H0	Time of Duty =32/32 : High Level Time = H*32t t is the period of PWMCLKDIV	RW	0x0
7:0	L0	Time of Duty =0/32 : Low Level Time = L*32t t is the period of PWMCLKDIV	RW	0x0

7.4.57 PWM1_CTL

PWM1 control register (RTCVDD) (default 0x0000)
Offset = 0x6E

Bit(s)	Name	Description	Access	Reset
15:8	H1	Time of Duty =32/32 : High Level Time = H*32t t is the period of PWMCLKDIV	RW	0x0
7:0	L1	Time of Duty =0/32 : Low Level Time = L*32t t is the period of PWMCLKDIV	RW	0x0

8 Auxiliary ADC

8.1 Module Description

ATC2603C integrates a 10-bit, 16-channel Analog-to-Digital Converter (ADC), which sample rate of each channel is 3.2kHz, converting one of the 16 analog inputs to 10-bit digital data. Its input voltage range is 0~3V, the application of each bit is listed below:

Table 8-1 AUXADC functional specifications

ADC_0	**ADC_1**	**ADC_2**	**ADC_3**	**ADC_4**	**ADC_5**	**ADC_6**	**ADC_7**
BATV	BATI	VBUSV	VBUSI	SYSPWRV	WALLV	WALLI	ICHG
ADC_8	**ADC_9**	**ADC_10**	**ADC_11**	**ADC_12**	**ADC_13**	**ADC_14**	**ADC_15**
SVCC/IREF	REM_CON	ICTEMP	BAKBAT	AUXADC0	AUXADC1	AUXADC2	ICMADC

AUXADC0~2 is for general use. WALL, SYSPWR and VBUS will pass a 2.5 voltage divider before sent to ADC, so the formula for WALL, SYSPWR, VBUS voltage (V) that relates their ADC output (DATA) can be described by:

$$V = DATA * LSB * 2.5$$

While BAT will pass a 2 voltage divider before sent to ADC, so the relationship between BAT voltage and its ADC output is:

$$V = DATA * LSB * 2$$

In addition, ADC also detects the current from VBUS to SYSPWR, current from BAT to SYSPWR, charger's charging current, BAKE BAT voltage, SVCC voltage, battery temperature and etc. The full current range of BATI, WALLI, VBUSI and ICHG current can be expressed as follows:

- $$IBAT = ADC\_DBG3 / IREFADC * 1545.75(mA)$$

$$IWALL = ADC\_DBG2 / IREFADC * 1527(mA)$$

$$IVBUS = ADC\_DBG1 / IREFADC * 1509(mA)$$

For CHIP_VER(0xDC)=0x0:

$$ICHG = ADC\_DBG0 / IREFADC * 1546(mA)$$

For CHIP_VER(0xDC)=0x1:

$$ICHG = ADC\_DBG0 / IREFADC * 2061(mA)$$

The relationship between IC Temperature (TEMP) and ICTEMP's ADC data can be expressed as follows:

$$TEMP = 0.1949 * DATA - 14.899 - 30(^{\circ}C)$$

For REM_CON ADC, its input range is 0~3V, the drive-by-wire ADC is distinguished by different voltages on different buttons. When the wire button's supply voltage is changed, the corresponding voltage of the same button will be different, so REM_CON data reflects the voltage ratio of REM_CON and SVCC:

$$REM\_CON = ADC\_DBG4 * 1024 / 2 * SVCCADC$$

In the formula above, ADC_DBG4*1024/2 represents different button's value, indicating that the button's voltage is ADC_DBG4*1024/2 times that of SVCC ADC, ADC_DBG4 is the REM_CON analog input value.

About the ICMADC:

Because a detection series resistor should be applied in the current detection route, so in case of large voltage drop, the detection resistor should be small. In this case, a pre-amplifier is implemented to amplify the small signal to the range of ADC input voltage. The input voltage range of ADC is 0~3V.

When an external 20mOhm resistor is used, the full range is -2312~+2312mA, accordingly, relationship between data and current is:

*I=DATA*LSBI = DATA * 2312/1024 (mA) = DATA*2.25832mA*

When an external 10mOhm resistor is applied, the full range is -4624~+4624mA, accordingly, relationship between data and current is:

*I=DATA*LSBI = DATA * 4624/1024 (mA) = DATA*4.51664 mA*

Note:

DATA is the decimal value of 0x50 PMU_ICADC[9:0]. PMU_ICADC[10] is the symbol bit, when it is 0 meaning forward current, flowing from CMN to CMP; when the current is negative, the absolute value calculated by ICMADC is larger 1 step than the actual value. For example, when 20mOhm is applied, if the actual current is -0.1mA, then the calculated value will be -2.25832mA.

8.2 Register List

Table 8-2 AUXADC Block Address

Name	Base Address
AUXADC	0x0000

Table 8-3 AUXADC Controller Registers

Offset	Register Name	Description
0x3E	PMU_AUXADC_CTL0	PMU AuxADC CONTROL Register0
0x3F	PMU_AUXADC_CTL1	PMU AuxADC CONTROL Register1
0x40	PMU_BATVADC	PMU BATVADC Register
0x41	PMU_BATIADC	PMU BATIADC Register
0x42	PMU_WALLVADC	PMU WALLVADC Register
0x43	PMU_WALLIADC	PMU WALLIADC Register
0x44	PMU_VBUSVADC	PMU VBUSVADC Register
0x45	PMU_VBUSIADC	PMU VBUSIADC Register
0x46	PMU_SYSPWRADC	PMU SYSPWRADC Register
0x47	PMU_REMCONADC	PMU REMCONADC Register

0x48	PMU_SVCCADC	PMU SVCCADC Register
0x49	PMU_CHGIADC	PMU CHGIADC Register
0x4A	PMU_IREFADC	PMU IREFADC Register
0x4B	PMU_BAKBATADC	PMU BAKBATADC Register
0x4C	PMU_ICTEMPADC	PMU ICTEMPADC Register
0x4D	PMU_AUXADC0	PMU AuxADC0 Register
0x4E	PMU_AUXADC1	PMU AuxADC1 Register
0x4F	PMU_AUXADC2	PMU AuxADC2 Register
0x70	PMU_ADC_DBG0	PMU ADC debug out0 register
0x71	PMU_ADC_DBG1	PMU ADC debug out1 register
0x72	PMU_ADC_DBG2	PMU ADC debug out2 register
0x73	PMU_ADC_DBG3	PMU ADC debug out3 register
0x74	PMU_ADC_DBG4	PMU ADC debug out4 register

8.3 Register Description

8.3.1 PMU_AUXADC_CTL0

PMU_AUXADC_CTL0 Register (RTCVDD) (default 0xFFFF)
Offset = 0x3E

Bit(s)	Name	Description	Access	Reset
15	AUXADC0_EN	AUXADC0 ADC enable 0: disable 1: enable	RW	1
14	AUXADC1_EN	AUXADC1 ADC enable 0: disable 1: enable	RW	1
13	AUXADC2_EN	AUXADC2 ADC enable 0: disable 1: enable	RW	1
12	ICMADC_EN	ICMADC ADC enable 0: disable 1: enable	RW	1
11	VBUSVADC_EN	VBUS VOLATGE ADC enable 0: disable 1: enable	RW	1
10	WALLVADC_EN	WALL VOLATGE ADC enable 0: disable 1: enable	RW	1
9	SYSPWRADC_EN	SYSPWR VOLATGE ADC enable 0: disable 1: enable	RW	1

8	BAKBATADC_EN	BAKBAT VOLTAGE ADC enable 0: disable 1: enable	RW	1
7	BATVADC_EN	BAT VOLATGE ADC enable 0: disable 1: enable	RW	1
6	TEMP_ADC	TEMP ADC enable 0: disable 1: enable	RW	1
5	REMCON_ADC_EN	REMCON ADC enable 0: disable 1: enable	RW	1
4	BATIADC_EN	BAT CURRENT ADC enable 0: disable 1: enable	RW	1
3	WALLIADC_EN	WALL CURRENT ADC enable 0: disable 1: enable	RW	1
2	VBUSIADC_EN	VBUS CURRENT ADC enable 0: disable 1: enable	RW	1
1	CHGIADC_EN	Charger current ADC enable 0: disable 1: enable	RW	1
0	IREFADC_EN/ SVCC_ADC_EN	CURRENT REF ADC enable/ SVCC ADC enable 0: disable 1: enable	RW	1

8.3.2 PMU_AUXADC_CTL1

PMU_AUXADC_CTL1 Register (RTCVDD) (default 0x000B)
Offset = 0x3F

Bit(s)	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11	CLK_EXT_SEL	Enable external clock, PMU_ADC adopt external clock input 1:enable 0:disable	RW	0
10	-	Reserved	-	-
9:8	AP_BIAS	Bias of coulomb meter's pre-amplifier: 00:0.5µA 01:medium	RW	01

		10 and 11:big		
7	EN_CM_AP	Enable coulomb meter's pre-amplifier 1:enable 0:disable	RW	1
6	ENCHOP	Enable pre-amplifier's primary offset reduction function 1:enable 0:disable	RW	1
5	AUTOGACTL_EN	Enable automatic gain control of the pre-amplifier. 1: gain = Auto Selection 0: gain = Fixed	RW	1
4	CM_R	The resistor between CMN and CMP 0:20mOhm 1:10mOhm	RW	0
3	ADC_COMP_TMEN	ADC Comp Offset Trimming 0: Disable 1: Enable	RW	1
2	ADC_COMP_BIAS	ADC COMP BIAS 0: 4μA1: bigger	RW	0
1	ADC_INPUT_RANGE	ADC INPUT RANGE 0: 0~1.5V 1: 0~3.0V	RW	1
0	ADC_CLOCK_ADJ	ADC clock adjust 0: 300kHz 1: higher	RW	1

8.3.3 PMU_BATVADC

PMU_BATADC Register (RTCVDD) (default 0x0000)
Offset = 0x40

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	BATVADC	BATVADC data	R	x

8.3.4 PMU_BATIADC

PMU_BATIADC Register (RTCVDD) (default 0x0000)
Offset = 0x41

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-

9:0	BATIADC	BATIADC data	R	x

8.3.5 PMU_WALLVADC

PMU_WALLADC Register (RTCVDD) (default 0x0000)
Offset = 0x42

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	WALLVADC	WALLVADC data	R	x

8.3.6 PMU_WALLIADC

PMU_WALLIADC Register (RTCVDD) (default 0x0000)
Offset = 0x43

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	WALLIADC	WALLIADC data	R	x

8.3.7 PMU_VBUSVADC

PMU_VBUSADC Register (RTCVDD) (default 0x0000)
Offset = 0x44

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	VBUSVADC	VBUSVADC data	R	x

8.3.8 PMU_VBUSIADC

PMU_VBUSIADC Register (RTCVDD) (default 0x0000)
Offset = 0x45

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	VBUSIADC	VBUSIADC data	R	x

8.3.9 PMU_SYSPWRADC

PMU_SYSPWRADC Register (RTCVDD) (default 0x0000)
Offset = 0x46

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	SYSPWRADC	SYSPWRADC data	R	x

8.3.10 PMU_REMCONADC

PMU_REMCONADC Register (RTCVDD) (default 0x0000)
Offset = 0x47

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	REMCONADC	REMCON ADC data	R	x

8.3.11 PMU_SVCCADC

PMU_SVCCADC Register (RTCVDD) (default 0x0000)
Offset = 0x48

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	SVCCADC	SVCC ADC data	R	x

8.3.12 PMU_CHGIADC

PMU_CHGIADC Register (RTCVDD) (default 0x0000)
Offset = 0x49

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	CHGIADC	CHGIADC data	R	x

8.3.13 PMU_IREFADC

PMU_IREFADC Register (RTCVDD) (default 0x0000)
Offset = 0x4A

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	IREFADC	IREFADC data	R	x

8.3.14 PMU_BAKBATADC

PMU_BAKBATADC Register (RTCVDD) (default 0x0000)
Offset = 0x4B

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	BAKBATADC	BAKE BATTERY VOLTAGE ADC data	R	x

8.3.15 PMU_ICTEMPADC

PMU_ICTEMPADC Register (RTCVDD) (default 0x0000)
Offset = 0x4C

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	ICTEMPADC	ICTEMPADC ADC data	R	x

8.3.16 PMU_AUXADC0

PMU_AuxADC0 Register (RTCVDD) (default 0x0000)
Offset = 0x4D

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	AUXADC0	AuxADC0 data	R	x

8.3.17 PMU_AUXADC1

PMU_AuxADC1 Register (RTCVDD) (default 0x0000)
Offset = 0x4E

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	AUXADC1	AUXADC1 data	R	x

8.3.18 PMU_AUXADC2

PMU_AuxADC2 Register (RTCVDD) (default 0x0000)
Offset = 0x4F

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	AUXADC2	AUXADC2 data	R	x

8.3.19 PMU_ADC_DBG0

PMU ADC debug 0 register (RTCVDD) (default 0x0000)
Offset = 0x70

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	ADC_DBG0	PMU ADC debug 0	R	x

8.3.20 PMU_ADC_DBG1

PMU ADC debug 1 register (RTCVDD) (default 0x0000)
Offset = 0x71

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	ADC_DBG1	PMU ADC debug 1	R	x

8.3.21 PMU_ADC_DBG2

PMU ADC debug 2 register (RTCVDD) (default 0x0000)
Offset = 0x72

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	ADC_DBG2	PMU ADC debug 2	R	x

8.3.22 PMU_ADC_DBG3

PMU ADC debug 3 register (RTCVDD) (default 0x0000)
Offset = 0x73

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	ADC_DBG3	PMU ADC debug 3	R	x

8.3.23 PMU_ADC_DBG4

PMU ADC debug 4 register (RTCVDD) (default 0x0000)
Offset = 0x74

Bit(s)	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:0	ADC_DBG4	PMU ADC debug 4	R	x

9 Real-Time Clock

9.1 Module Description

RTC module provides system timing and alarm functions, it supports power-off and power-on by alarm. Its clock is based on 32.768 kHz oscillator, which can be provided by a built-in or external oscillator, and the external OSC is used by default.
At the system power on the internal OSC is used, then there is a process of selecting clock source, if an oscillatory waveform is detected at LOSC, the detect circuit will delay about 1ms and then set RTC_CTL[3] to 1, and external OSC is selected. If no waveform is detected at LOSC, the detect circuit will delay about 3ms and set RTC_CTL[3] to 0, internal OSC will be selected.
Whether the system is in Standby or normal working mode, if the system chooses the external LOSC but the external LOSC stopped working, RTCVDD_OK will be pulled down and then the whole system will be reset. Powered on next time, the system will use internal OSC by default.

9.1.1 32kHz Oscillator

An external 32.768 kHz crystal oscillator should be supplied to ATC2603C system to get an accurate clock for Real Time Clock (RTC) and an alarm function capable of waking up the system. If the requirement for 32.768 kHz clock is not too accurate, the system will choose the built-in oscillator instead of the external 32.768 kHz oscillator.

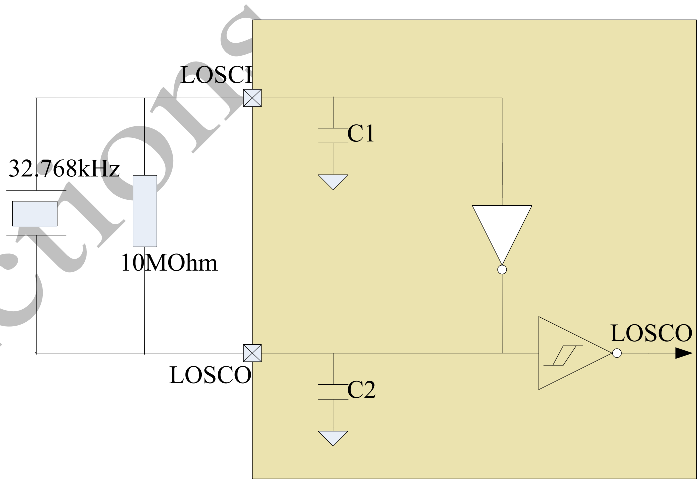


Figure 9-1 LOSC block diagram

The main clock of ATC2603C is got directly from the Master.

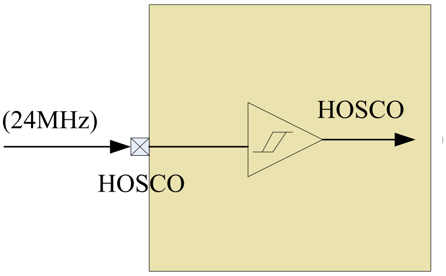


Figure 9-2 HOSC block diagram

9.1.2 Calendar

When RTCE=1, RTC_H, RTC_MS and RTC_YMD clock is based on LOSC_CLK, Master can only read the registers to get the current time in this case. When RTCE=0, the registers can be written to set the current time.

9.1.3 Alarm

When RTCE=ALIE=1, if RTC_HALM=RTC_H, RTC_MSALM=RTC_MS and RTC_YMDALM = RTC_YMD, an Alarm IRQ will be generated, which can be cleared by setting ALIP to 1.

9.2 Register List

Table 9-1 RTC Block Address

Name	Base Address
RTC	0x0000

Table 9-2 RTC Controller Registers

Offset	Register Name	Description
0x52	RTC_CTL	RTC control register
0x53	RTC_MSALM	RTC ALARM Minute second REGISER
0x54	RTC_HALM	RTC ALARM Hour REGISER
0x55	RTC_YMDALM	RTC ALARM Year month date REGISER
0x56	RTC_MS	RTC Minute second REGISER
0x57	RTC_H	RTC Hour REGISER
0x58	RTC_DC	RTC day century REGISER
0x59	RTC_YMD	RTC year month date REGISER

9.3 Register Description

9.3.1 RTC_CTL

Calendar Control Register (RTCVDD) (default 0x5A50)

Offset=0x052

Bits	Name	Description	Access	Reset
15:14	LGS	Low frequency crystal Oscillator GMNIN select bits	RW	1
13:12	LOSC_CP	LOSC Capacitor Select: 00:12pF 01:15pF 10:18pF 11:21pF	RW	1
11	RST	RTC Reset 1: Normal 0: Reset	RW	1
10	VERI	RTC Verify Clock Enable Switch RTC clock to 32 kHz 1: Enable 0: Disable	RW	0
9	LEAP	RTC Leap Year bit 1: leap year 0: non-leap year	R	1
8:7	-	Reserved	-	-
6	EOSC	External Crystal OSC enable 1: Enable 0: Disable	RW	1
5	CKSS0	RTC_32K clock Source Select 1: External Crystal OSC 0: Built-in OSC	RW	0
4	RTCE	RTC Enable 1: Enable 0: Disable	RW	1
3	EXT_LOSC_STATE	External LOSC State: 0:external LOSC stop Oscillating 1:external LOSC is Oscillating	R	x
2	-	Reserved	-	-
1	ALIE	Alarm IRQ Enable 1: Enable 0: Disable	RW	0
0	ALIP	Alarm IRQ Pending bit, writing 1 to this bit will clear it	RW	0

Note:

- Bit[5] CKSS0: only when RTCVDD is completely powered off, will CKSS0 be reset.
- Calendar and Alarm module need precise low frequency clock, so an external crystal OSC is should be applied in application.
- Bit[13:12] LOSC_CP: LOSC circuit matching capacitor selection should refer to the load capacitor of the external crystal OSC, a default value of 01 or 10 is used in general.
- Bit[15:14] LGS: this bit is the LOSC circuit driving ability enhancing bit, the driving strength can be sorted as 2b11>2b10>2b01>2b00, the default value is recommended.
- Bit[3] EXT_LOSC_STATE: the state bit of external starting LOSC oscillating.

9.3.2 RTC_MSALM

Calendar MSALM Register (RTCVDD) (default 0x0000)
Offset=0x053

Bits	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:6	MINAL	Alarm minute setting 0x00 – 0x3B	RW	0
5:0	SECAL	Alarm second setting 0x00 – 0x3B	RW	0

9.3.3 RTC_HALM

Calendar HALM Register (RTCVDD) (default 0x0000)
Offset=0x054

Bits	Name	Description	Access	Reset
15:5	-	Reserved	-	-
4:0	HOUEAL	Alarm hour setting 0x00 – 0x17	RW	0

9.3.4 RTC_YMDALM

Calendar YMDALM Register (RTCVDD) (default 0x0000)
Offset=0x055

Bits	Name	Description	Access	Reset
15:9	YEARAL	Alarm year setting 0x00 – 0x63	RW	0
8:5	MONAL	Alarm month setting 0x01 – 0x0C	RW	0
4:0	DATEAL	Alarm day setting 0x01 – 0x1F	RW	0

9.3.5 RTC_MS

Calendar MS Register (RTCVDD) (default 0x0000)
Offset=0x056

Bits	Name	Description	Access	Reset
15:12	-	Reserved	-	-
11:6	MIN	Time minute setting 0x00 – 0x3B	RW	0
5:0	SEC	Time second setting 0x00 – 0x3B	RW	0

9.3.6 RTC_H

Calendar HOUR Register (RTCVDD) (default 0x0000)
Offset=0x057

Bits	Name	Description	Access	Reset
15:5	-	Reserved	-	-
4:0	HOUR	Time hour setting 0x00 – 0x17	RW	0

9.3.7 RTC_DC

Calendar DC Register (RTCVDD) (default 0x0080)
Offset=0x058

Bits	Name	Description	Access	Reset
15:10	-	Reserved	-	-
9:7	DAY	Time day setting 0x01 – 0x07	RW	1
6:0	CENT	Time setting 0x00 – 0x63	RW	0

9.3.8 RTC_YMD

Calendar YMD Register (RTCVDD) (default 0x0021)
Offset=0x059

Bits	Name	Description	Access	Reset
15:9	YEAR	Time year setting 0x00 – 0x63	RW	0
8:5	MON	Time month setting 0x01 – 0x0C	RW	1

4:0	DATE	Time day setting 0x01 – 0x1F	RW	1

10 Infrared Remote Controller

10.1 Features

ATC2603C Infrared Remote Controller (IRC) module Support RC5/9012/NEC(8-bit)/RC6 protocol, the sample clock is 32.576kHz. IRC is connected with an Infrared Remote (IR) receiver, only when the received key data is equal to the IRC_WK register's data, including NEC, 9012, RC5 and RC6 mode, can IRC wake up the system by generating a wake up signal to PMU.

10.2 Modules Description

10.2.1 9012 Protocol

The 9012 protocol adopts PDM (Pulse Distance Modulation). Each pulse is one Tm (560µs) 38kHz carrier burst, and LSB is transmitted first. Logic 1 takes 4Tm (2.25ms) to transmit, and logic 0 only takes 2Tm (1.12ms). A message is started by 8Tm (4.5ms) AGC burst, used to set the gain of the front IR receivers. Customer code and Command code length is both 8-bit, and they are transmitted twice to ensure the reliability of the transmission. And in the second time, Command code is inverted to Anti-code to verify the received messages.

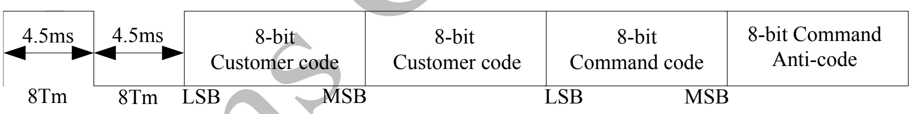


Figure 10-1 9012 Protocol of Frame

Below are some values for reference:

Recommended carrier duty-cycle = 1/4 or 1/3.

Tm = 256/Fosc = 0.56ms (Fosc=455kHz)

Repetition time = 192Tm = 108ms

Carrier frequency = Fosc/12

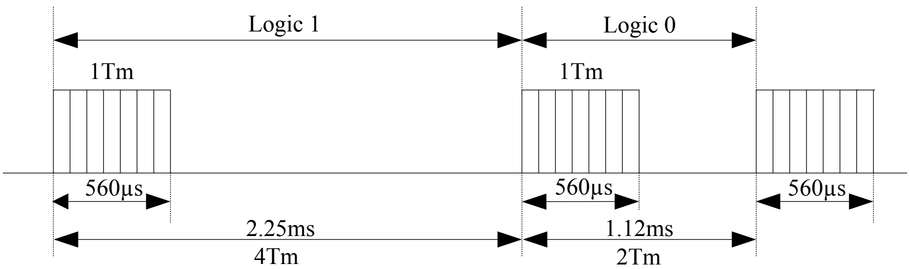


Figure 10-2 9012 Protocol of Logic transmission

When the key on the remote controller remains pressed down, the command will be transmitted only once, even a repeat code is transmitted every 192Tm as long as the key remains pressed down. This repeat code is 8Tm (4.5ms) AGC pulse followed by 8Tm (4.5ms) space and a logic 1 plus 1Tm (560µs) burst.

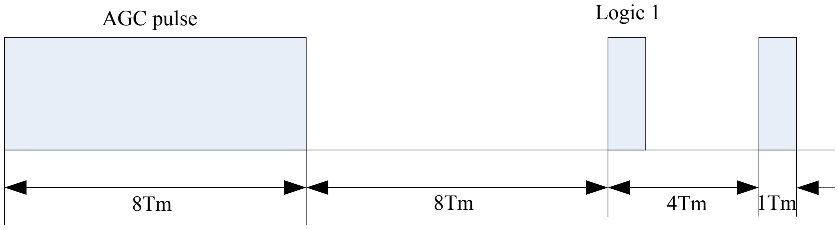


Figure 10-3 9012 Protocol of Repeat Code

10.2.2 NEC Protocol (8-bit)

The NEC protocol adopts Pulse Distance Modulation. Each pulse is one Tm (560µs) 38kHz carrier burst, and LSB is transmitted first. Logic 1 takes 4Tm (2.25ms) to transmit, logic 0 only takes 2Tm (1.12ms). A message is started by 16Tm (9ms) AGC burst, which was used to set the gain of the front IR receivers. This AGC burst is followed by 8Tm (4.5ms) space, and then the Customer and Command code. Customer and Command codes are both 8-bit, they are transmitted twice for reliability; the second customer and command code are inverted to Anti-code to verify the received message. The whole transmission time is constant because every bit is repeated with its inverted length.

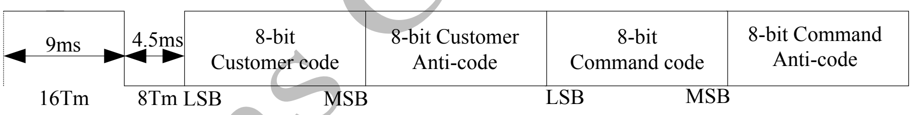


Figure 10-4 NEC Protocol of Frame

Below are some values for reference:

Recommended carrier duty-cycle: 1/4 or 1/3

Tm = 256/Fosc = 0.56ms (Fosc=455kHz)

Repetition time = 192Tm = 108ms

Carrier frequency = Fosc/12

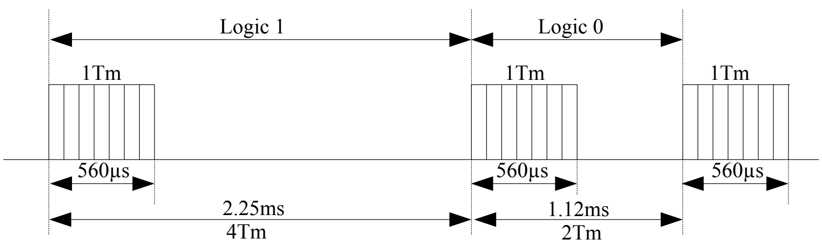


Figure 10-5 NEC Protocol of Logic transmission

When the key on the remote controller remains pressed down, the command will be transmitted only once, even a repeat code is transmitted every 192Tm as long as the key remains pressed down. This repeat code is a 16Tm (9ms) AGC pulse followed by a 4Tm (2.25ms) space and a Tm (560µs) burst.

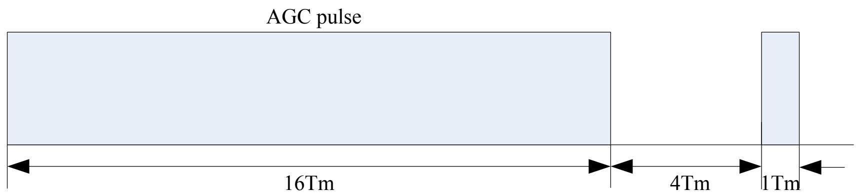


Figure 10-6 NEC Protocol Repeat Code

10.2.3 RC5 Protocol

The RC5 protocol adopts Bi-phase Modulation (or Manchester coding) of 38kHz IR carrier frequency. Transmission time of each bit is 1.8ms in this protocol, in which half of the transmission time is for the 38kHz carrier and the other half being idle. Logic 0 is a burst in the first half of the transmission time, logic 1 is a burst of the second half of the transmission time; see in Figure 10-7 below. The pulse/pause ratio of the 38kHz carrier frequency is 1/3 or 1/4, which reduced the power consumption.

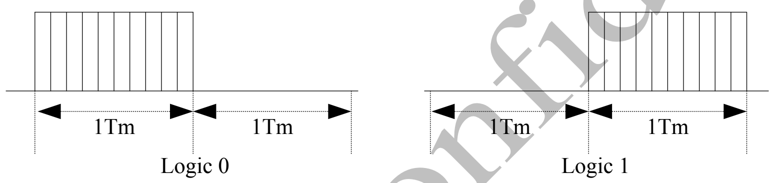


Figure 10-7 RC5 Protocol Logic

Below are some values for reference:

1 bit-time = 3*256 /Fosc= 1.688ms (Fosc=455kHz)

Tm= 1 bit-time/2=0.844ms

Repetition time= 4*16*2Tm=108ms

Carrier frequency = Fosc/12

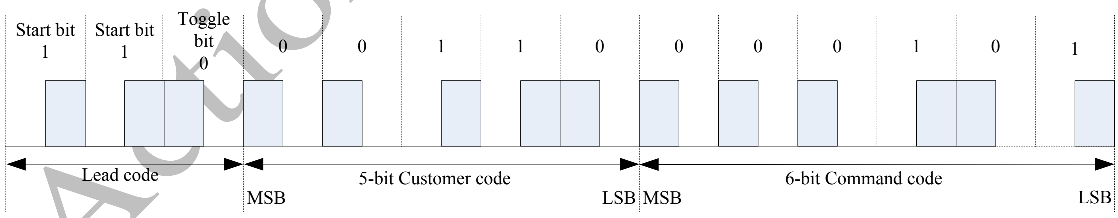


Figure 10-8 RC5 Protocol Frame

The first two pulses are start pulses, both are logic 1. Half of the transmission time will be elapsed before the receiver recognizes the real start of the message. The third bit is a toggle bit, this bit is inverted every time a key is released and pressed again. This is how the receiver distinguishes whether the key remains pressed down or repeatedly pressed. The next 5-bit Customer code represents the IR device's address, with MSB sent first. The following 6-bit command code is sent with MSB first, too. One message is 14 bits in total, which adds up to time duration of 28Tm. Sometimes a message may be shorter because the first half of the start bit S1 is idle, and if the last bit of the message is logic 0 the last half bit of the message is idle too. As long as a key remains down the message will be repeated every 128Tm (108ms). The toggle bit will remain the same logic during these repeated messages. And this auto repeat feature can be configured by the receiver software.

Figure 10-9 RC5 Protocol of Repetition time

10.2.4 RC6 Protocol

The RC6 Protocol of mode 0 is supported only. RC-6 signals are modulated on a 36 kHz Infrared Red carrier. The duty cycle of this carrier is recommended between 25% and 50%. Transmission data is modulated using Manchester coding. This means that each bit (or symbol) will have both a mark and space in the output signal. If the symbol is 1, the first half of the bit time is a mark and the second half is a space. If the symbol is 0, the first half of the bit time is a space and the second half is a mark.

The main timing unit is 1T, which is 16 times the carrier period (1/36kHz * 16 = 444µs)

1T =1*16 / 36kHz = 444µs

1Bit = 2T = 888µs

Total transmission time (22 Bits) = 23.1ms(message) + 2.7ms (no signal)

Repetition time = 240T = 106.7ms

LS	SB	mb2 ... mb0	TR	a7 ... a0	c7 .... c0	
Header				Control	Information	Signal free

Figure 10-10 RC6 Protocol

The RC6 Protocol frame can be separated into four fields: Header, Control, Information and Signal free field. The signal free field is not used.

Header Field:

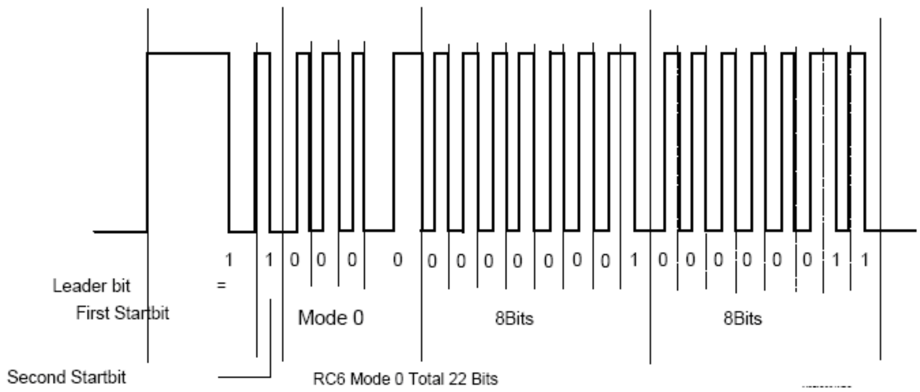


Figure 10-11 RC6 Protocol of Signal Frame

This leader bit is the start bit used to set the gain of the IR receiver unit, which has a mark time of 6T (2.666ms) and a space time of 2T (0.889ms).

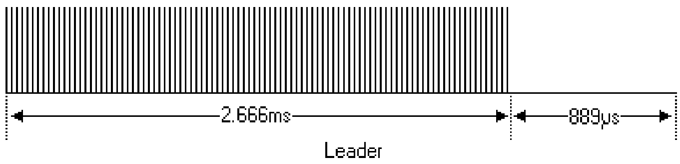


Figure 10-12 RC6 Protocol of Leader Bit

The normal bit, 0 and 1 are encoded by the position of the mark and space in the bit time, in which mark time is1T (0.444ms) and space time is1T (0.444ms).

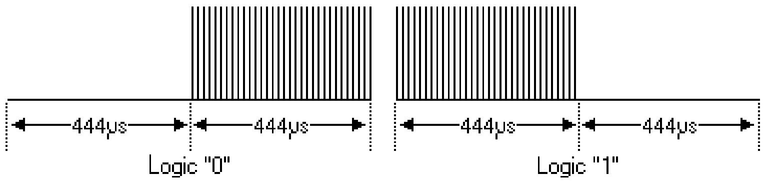


Figure 10-13 RC6 Protocol of Normal Bit

The trailer bit TR has a mark time of 2T (0.889ms) and a space time of 2T (0.889ms). Same, 0 and 1 are encoded by the position of the mark and space in the bit time. This bit functions like the traditional toggle bit, which will be inverted whenever a key is released. This bit separates a long key-press from a double key-press.

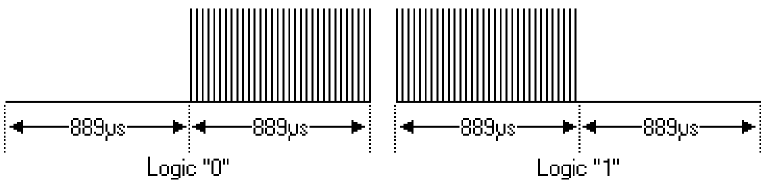


Figure 10-14 RC6 Protocol of Trailer Bit

Control field:

This field holds 8 bits which are used as address byte. This means that a total of 256 different devices can be controlled using mode 0 of RC-6. The MSB is transmitted first.

Information field:

The information field holds 8 bits which are used as command byte. This means that each device can have up to 256 different commands. The MSB is transmitted first.

10.3 Register List

Table 10-1 IRC Block Address

Name	Base Address
IRC	0x0000

Table 10-2 IRC Controller Registers

Offset	Register Name	Description
0x80	IRC_CTL	Infrared remote control register
0x81	IRC_STAT	Infrared remote status register
0x82	IRC_CC	Infrared remote control customer code register
0x83	IRC_KDC	Infrared remote control KEY data code register

0x84	IRC_WK	Infrared remote control wake up KEY data code register
0x85	IRC_RCC	Infrared remote control Receive customer code register
0x86	IRC_FILTER	Infrared remote control Filter register

10.4 Register Description

10.4.1 IRC_CTL

Infrared remote control register (RTCVDD) (default 0x0000)
Offset = 0x80

Bit(s)	Name	Description	Access	Reset
15:4	-	Reserved	-	-
3	IRE	IRC enable 0: disable 1: enable	RW	0x0
2	IIE	IRC IRQ enable 0: disable 1:enable	RW	0x0
1:0	ICMS	IRC code mode select 00: 9012 code 01: 8bits NEC code 10: RC5 code 11: RC6 code	RW	0x0

10.4.2 IRC_STAT

Infrared remote control register (RTCVDD) (default 0x0000)
Offset = 0x81

Bit(s)	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6	UCMP	User code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct user code the next time. 0: user code match 1: user code don't match	RW	0x0
5	KDCM	Key data code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct key data code the next time 0: key data code match 1: key data code don't match	RW	0x0
4	RCD	Repeated code detected, write 1 to this bit will clear it,	RW	0

		otherwise don't change 0: no repeat code 1: detect repeat code		
3	-	Reserved	-	-
2	IIP	IRC IRQ pending bit, write 1 to this bit will clear it 0: no IRQ pending 1: IRQ pending The precondition of generating interrupt is that all the code received is correct, including customer code and key code. If neither customer code nor key code is incorrect, the repeat code following this frame won't generate interrupt, too.	RW	0x0
1	-	Reserved	-	-
0	IREP	IRC receive error pending 0: receive OK 1: receive error occurs if not match the protocol. Writing 1 to this bit will clear this bit, or auto clear if receive the correct user code and key data code the next time.	RW	0x0

10.4.3 IRC_CC

Infrared remote control customer code register (RTCVDD) (default 0x0000)
Offset = 0x82

Bit(s)	Name	Description	Access	Reset
15:0	ICCC	Infrared remote control customer code **In RC5 mode:** Bit 4:0 is the customer code; **In 9012 and NEC mode:** Bit 15:0 is the customer code; **In RC6 mode:** Bit 7:0 is the customer code; If the received customer codes not comply with this register value, error occurs.	RW	0x0

10.4.4 IRC_KDC

Infrared remote control KEY data code register (RTCVDD) (default 0x0000)
Offset = 0x83

Bit(s)	Name	Description	Access	Reset
15:0	IKDC	IRC key data code **In RC5 mode:**	RW	0x0

		Bit 5:0 is the Key data; **In 9012 and NEC mode:** Bit 7:0 is the Key data; Bit 15:8 is the Key anti-data; **In RC6 mode:** Bit 7:0 is the Key data; Once the key value is received the register will be updated, if repeat code is received, then the register won't be updated.		

10.4.5 IRC_WK

Infrared remote control wake up KEY data code register (RTCVDD) (default 0x0000)
Offset = 0x84

Bit(s)	Name	Description	Access	Reset
15:0	IKDC	IRC wake up key data code **In RC5 mode:** Bit 5:0 is the wake up Key data; **In 9012 and NEC mode:** Bit15:0 is the wake up key data; Bit 7:0 is the Key data; Bit 15:8 is the Key anti-data; **In RC6 mode:** Bit 7:0 is the wake up key data; If the received key value is not same with the value set by this register, then a wakeup signal will be generated to PMU, and an interrupt will be generated at the same time.	RW	0x0

10.4.6 IRC_RCC

Receive customer code register (RTCVDD) (default 0x0000)
Offset = 0x85

Bit(s)	Name	Description	Access	Reset
15:0	ICCC	Received customer code **In RC5 mode:** Bit 4:0 is the customer code; **In 9012 and NEC mode:** Bit 15:0 is the customer code; **In RC6 mode:** Bit 7:0 is the customer code; The received customer code is displayed to	R	0x0

		customers for reference.		

10.4.7 IRC_FILTER

Infrared remote control filter register (RTCVDD) (default 0x0000)
Offset = 0x86

Bit(s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	FC	IR Filter control bit 0: disable 1: enable	RW	0x0
2:0	IFC	IR filter counter Determine the pulse width that can be filtered. 32.768kHz clock source cycle number, each cycle is 30.517us. Here one cycle is a unit, for example, setting T = 20us, then write 6 (200/30.517) to this register	RW	0x0

11 Interrupt Controller

11.1 Features

Interrupt Controller (INTS) module can receive and handle 16 Interrupt signals sent through pin EXTIRQ. Table 11-1 lists all the interrupt sources. Details about these interrupts can be found in relevant sections. Please refer to the register INTS_PD to get interrupt that has happened, besides, any of these 16 interrupts can be masked by setting register INTS_MSK.

Table 11-1 Interrupt Sources list

Interrupt Number	Sources	Type
0	AUDIO	High Level
1	OV	High Level
2	OC	High Level
3	OT	High Level
4	UV	High Level
5	ALARM	High Level
6	ONOFF	High Level
7	SGPIO	High Level
8	IR	High Level
9	REMCON	High Level
10	POWERIN	High Level
11-15	Reserved	-

Note: OV-overvoltage, OC-overcurrent, OT-overtemperature, UV-Undervoltage.

11.2 Block Diagram

Figure 11-1 given below shows the architecture of the interrupt controller:

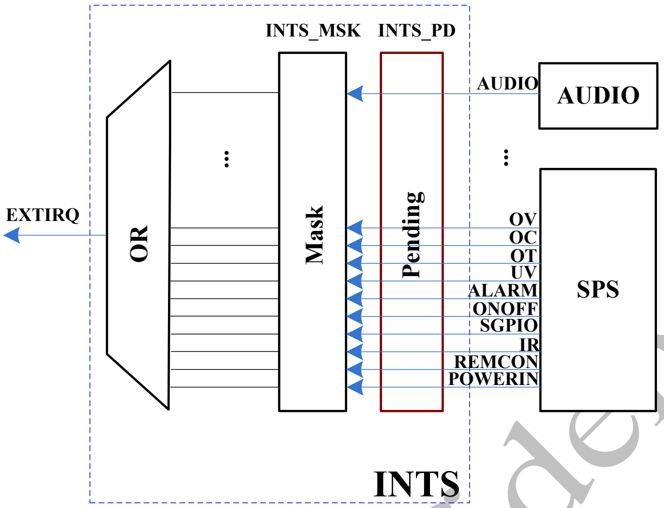


Figure 11-1 Interrupt Controller Block Diagram

11.3 Register List

Table 11-2 Interrupt source Block Base Address

Name	Base Address
INTS_REGISTER	0xC8

Table 11-3 Interrupt source Block Configuration Registers List

Offset	Register Name	Description
0x00	INTS_PD	Interrupt Pending register
0x01	INTS_MSK	Interrupt Mask register

11.4 Register Description

11.4.1 INTS_PD

CPU can access the status of interrupt sources by read this register. Interrupt Pending bit can not be cleared by writing 1, it is not cleared until device pending is cleared.
offset = 0x00

Bit	Name	Description	Access	Reset
15:11	-	Reserved	-	-
10:0	INTS_PD	Interrupt Pending bit. Interrupt name “n”	R	INTS_PD[n]

		please refer to Interrupt Sources Table. 0: Interrupt source n request is not active 1: Interrupt source n request is active.		

11.4.2 INTS_MSK

CPU can enable or disable by write this register. 0: Interrupt is disabled. 1: Interrupt is enabled.
offset = 0x01

Bits	Name	Description	Access	Reset
15:11	-	Reserved	-	-
10	POWERIN	POWER IN Interrupt Mask Bit	RW	0
9	REMCON	REMOTE CONTROL Interrupt Mask Bit	RW	0
8	IR	IR Interrupt Mask Bit	RW	0
7	SGPIO	SGPIO Interrupt Mask Bit	RW	0
6	ONOFF	ONOFF Interrupt Mask Bit	RW	0
5	ALARM	ALARM Interrupt Mask Bit	RW	0
4	UV	UN-VOLTAGE Interrupt Mask Bit	RW	0
3	OT	OVER TEMPERATURE Interrupt Mask Bit	RW	0
2	OC	OVER CURRENT Interrupt Mask Bit	RW	0
1	OV	OVER VOLTAGE Interrupt Mask Bit	RW	0
0	AUDIO	AUDIO Interrupt Mask Bit	RW	0

12 General Purpose I/O

12.1 Features

This chapter will describe the multiplexing of the whole system and the GPIO function. There are 8 bits General purpose I/O ports in ATC2603C to provide more flexible application. The 8 GPIOs have independent inputs and outputs, and the multiplexing is software controlled and can be configured for different applications. The GPIOs support different driving capacities.

12.2 Registers List

Table 12-1 GPIO/MFP Registers Block base Address

Name	Base Address
MFP_REGISTER	0xD0

Table 12-2 GPIO/MFP Registers Offset Address

Offset	Register Name	Description
0x00	MFP_CTL	Multiplexing Control
0x02	GPIO_OUTEN	GPIO Output Enable
0x03	GPIO_INEN	GPIO Input Enable
0x04	GPIO_DAT	GPIO Data
0x05	PAD_DRV	PAD Drive Capacity Select
0x06	PAD_EN	PAD enable control

12.3 Register Description

12.3.1 MFP_CTL

Multiplexing Control Register
Offset=0x00

Bits	Name	Description	Access	Reset
15:13	-	Reserved	-	-
12:11	MICINR	MICINR multiplexing 00: MICINR 01: MICINLP (or MICINRP) 10: Reserved 11:Reserved	RW	0x0
10:9	FMINL_R	FMINL and FMINR multiplexing 00: FMINL, FMINR 01: Reserved 10: MICINLP 11: Reserved (This pad is analog and digital multiplexed)	RW	0x0
8:7	I2S_MCLK1_LRCLK1_DOUT	I2S_MCLK1, I2S_LRCLK1, I2S_DOUT Multiplexing 00: I2S_MCLK1, I2S_LRCLK1 and I2S_DOUT 01: GPIO3, GPIO4 and GPIO5 10: LOSC_32K, LOSC_32K and I2S_DOUT 11: Reserved	RW	0x0
6:5	I2S_MCLK0_LRCLK0	I2S_MCLK0 and I2S_LRCLK0 Multiplexing 00: I2S_MCLK0 and I2S_LRCLK0 01: GPIO0 and GPIO1 10: Reserved 11: Reserved	RW	0x0

4:3	I2S_DIN	I2S_DIN Multiplexing 00: I2S_DIN 01: GPIO2 10: I2S_DOUT 11: Reserved	RW	0x0
2	-	Reserved	-	-
1:0	MICINL	MICINL multiplexing 00: MICINL 01: MICINLN(or MICINRN) 10: Reserved 11: Reserved	RW	0x0

Note: When bit[1:0] and bit[12:11]is set to 01, Choosing (MICINLN and MICINLP) or (MICINRN and MICINRP) is determined by MICEN & ADCEN.

12.3.2 GPIO_OUTEN

GPIO Output Enable Register
Offset=0x02

Bits	Name	Description	Access	Reset
15:6	-	Reserved	-	-
5:0	GPIO_OUTEN	GPIO[5:0] Output Enable. 0: Disable 1: Enable	RW	0x0

12.3.3 GPIO_INEN

GPIO Input Enable Register
Offset=0x03

Bits	Name	Description	Access	Reset
15:6	-	Reserved	-	-
5:0	GPIO_INEN	GPIO[5:0] Input Enable. 0: Disable 1: Enable	RW	0x0

12.3.4 GPIO_DAT

GPIO Data Register
Offset=0x04

Bits	Name	Description	Access	Reset

15:6	-	Reserved	-	-
5:0	GPIO_DAT	GPIO[5:0] Input/Output Data.	RW	0x0

12.3.5 PAD_DRV

Pad Driving Capacity
Offset=0x05

Bits	Name	Description	Access	Reset
15:14	-	Reserved	-	-
13	EXTIRQ_DRV	PAD EXTIRQ Drive Capacity 0: Level 1 1: Level 2	RW	0x0
12	TWSI_CLK_DATA_DRV	PAD TWSI_CLK&TWSI_DATA Drive Capacity 0: Level 1 1: Level 2	RW	0x0
11:10	I2S_MCLK1_DRV	PAD I2S_MCLK1 Drive Capacity 0:Level 1 1:Level 3 2:Level 5 3:reserved	RW	0x0
9:8	I2S_LRCLK1_DRV	PAD I2S_LRCLK1 Drive Capacity 0:Level 1 1:Level 3 2:Level 5 3:reserved	RW	0x0
7:6	I2S_MCLK0_DRV	PAD I2S_MCLK0 Drive Capacity 0:Level 1 1:Level 3 2:Level 5 3:reserved	RW	0x0
5:4	I2S_LRCLK0_DRV	PAD I2S_LRCLK0 Drive Capacity 0:Level 1 1:Level 3 2:Level 5 3:reserved	RW	0x0
3:2	I2S_DOUT_DRV	PAD I2S_DOUT Drive Capacity 0:Level 1 1:Level 3 2:Level 5 3:reserved	RW	0x0
1:0	I2S_DIN_DRV	PAD I2S_DIN Drive Capacity	RW	0x0

		0:Level 1 1:Level 3 2:Level 5 3:reserved		

12.3.6 PAD_EN

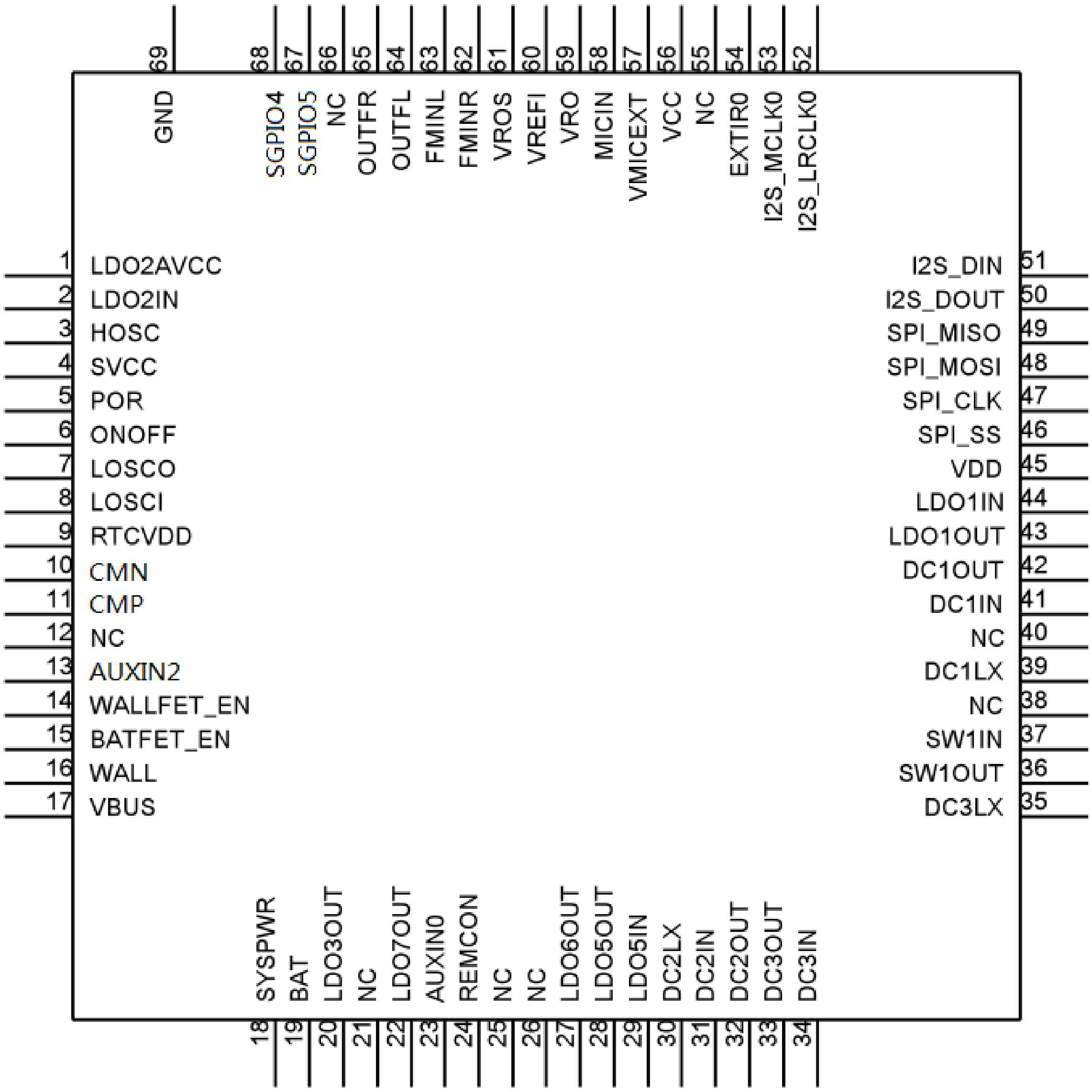
Pad enable control

Offset=0x06

Bits	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6	PAD_EN6	1:P_I2S_MCLK0 pad enable 0:P_I2S_MCLK0 pad disable	RW	0x0
5	PAD_EN5	1:P_I2S_LRCLK0 pad enable 0:P_I2S_LRCLK0 pad disable	RW	0x0
4	PAD_EN4	1:P_I2S_DIN pad enable 0:P_I2S_DIN pad disable	RW	0x0
3	PAD_EN3	1:P_I2S_MCLK1 pad enable 0:P_I2S_MCLK1 pad disable	RW	0x0
2	PAD_EN2	1:P_I2S_LRCLK1 pad enable 0:P_I2S_LRCLK1 pad disable	RW	0x0
1	PAD_EN1	1:P_I2S_DOUT pad enable 0:P_I2S_DOUT pad disable	RW	0x0
0	PAD_EN0	1:P_EXTIRQ pad enable 0:P_EXTIRQ pad disable	RW	0x0

13 Pin Description

13.1 ATC2603C Pin Assignment



Note: This is a schematic figure for ATC2603C, Pin 69 is e-pad under the IC

Figure 13-1 ATC2603C schematic pin assignment

13.2 ATC2603C Pin Definition

Table 13-1 ATC2603C Pin descriptions

Pin No.	Pin Name	Function Name	I/O	Description
1	LDO2AVCC	LDO2AVCC	power	Output of voltage regulator LDO2, also for Analog IO use

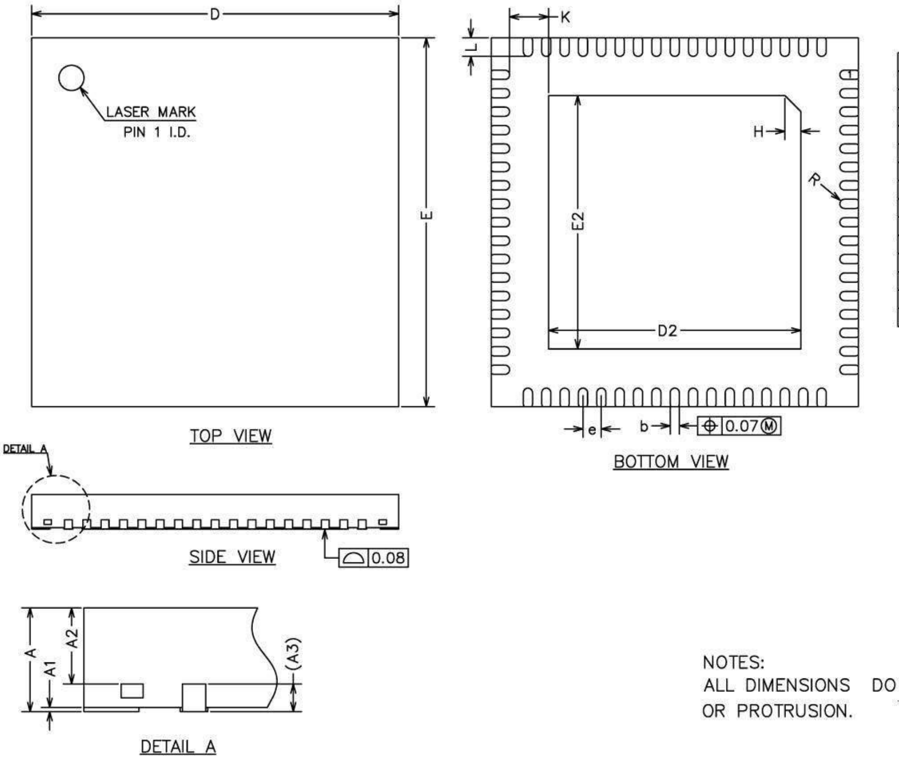
2	LDO2IN	LDO2_8IN	supply	Input of voltage regulator LDO2
3	HOSC	HOSCO	AO	Connection for 24 MHz crystal (input to oscillator from crystal)
4	SVCC	SVCC	power	Output of voltage regulator LDO11, the IO power for standby mode
5	POR	POR	DO	power on reset output to main controller
6	ONOFF	ONOFF	DI	ONOFF key input/reset signal
7	LOSCO	LOSCO	AIO	Crystal Oscillator Input of 32.768 kHz
8	LOSCI	LOSCI	AI	Crystal Oscillator output of 32.768 kHz
9	RTCVDD	RTCVDD	power	Output of voltage regulator LDO12
10	CMN	CMN	AIO	CM ADC input
11	CMP	CMP	AIO	CM ADC input
12	NC	-	-	-
13	AUXIN2	AUXIN2 IR LOSC_32K	AIO	general ADC input2 IR control input 32K clock output
		SGPIO3	DIO	General Purpose Input/Output 3 SVCC
14	WALLFET_EN	WALLFET_EN	AO	Gate signal of external MOSFET connected to WALL
15	BATFET_EN	BATFET_EN	AO	Gate signal of external MOSFET connected to BAT
16	WALL	WALL	supply	Connected to wall adapter power supply
17	VBUS	VBUS	supply	Connected to USB power supply
18	SYSPWR	SYSPWR	power	SYSTEM POWER
19	BAT	BAT	supply	Connected to battery power supply
20	LDO3OUT	LDO3OUT	power	Core logic power
21	NC	-	-	-
22	LDO7OUT	LDO7OUT	AO	Output of voltage regulator LDO7
23	AUXIN0	AUXIN0 IR LOSC_32K PWM0	AIO	general ADC input0 IR control input 32K clock output PWM output0
		SGPIO1	DIO	General Purpose Input/Output 1 SVCC
24	REMCON	REM_CON IR LOSC_32K	AIO	general ADC input4, for remote control IR control input 32K clock output
		SGPIO0	DIO	General Purpose Input/Output 0 SVCC
25	NC	-	-	-
26	NC	-	-	-
27	LDO6OUT	LDO6OUT	AO	Output of voltage regulator LDO6
28	LDO5OUT	LDO5OUT	AO	Output of voltage regulator LDO5
29	LDO5IN	LDO5IN	supply	Input of voltage regulator LDO5

30	DC2LX	DC2LX	AO	DC-DC2 inductor connection
31	DC2VIN	DC2VIN	supply	DC-DC2 power input
32	DC2VOUT	DC2VOUT	AO	Output of DC-DC2
33	DC3VOUT	DC3VOUT	power	Output of DC-DC3
34	DC3VIN	DC3VIN	supply	DC-DC3 power input
35	DC3LX	DC3LX	AO	DC-DC3 inductor connection
36	SWITCH1OUT	SWITCH1OUT	power	Output of voltage regulator Switch1
37	SWITCH1IN	SWITCH1IN	supply	Input of voltage regulator Switch1
38	NC	-	-	-
39	DC1LX	DC1LX	AO	DC-DC1 inductor connection
40	NC	-	-	-
41	DC1VIN	DC1VIN	supply	DC-DC1 power input
42	DC1VOUT	DC1VOUT	power	Output of DC-DC1
43	LDO1OUT	LDO1OUT	AO	Output of voltage regulator LDO1
44	LDO1IN	LDO1IN	supply	Input of voltage regulator LDO1&LDO10
45	VDD	VDD	power	Core logic power
46	I2S_LRCLK1	I2S_LRCLK1 LOSC_32K GPIO4	DI	I2S LR CLOCK1 32K clock output General Purpose Input/Output 4
47	TWI_SCLK	TWI_SCLK	DI	TWI clock
48	TWI_SDATA	TWI_SDATA	DI	TWI data
49	I2S_MCLK1	I2S_MCLK1 LOSC_32K GPIO3	DO	I2S Master CLOKCK1 32K clock output General Purpose Input/Output 3
50	I2S_DOUT	I2S_DOUT GPIO5	DIO	I2S DATA output General Purpose Input/Output 5
51	I2S_DIN	I2S_DIN I2S_DOUT GPIO2	DIO	I2S Data input I2S Data output General Purpose Input/Output 2
52	I2S_LRCLK0	I2S_LRCLK0 GPIO1	DIO	I2S LR CLOCK0 General Purpose Input/Output 1
53	I2S_MCLK0	I2S_MCLK0 GPIO0	DIO	I2S Master CLOKCK0 General Purpose Input/Output 0
54	EXTIRQ	EXTIRQ	DO	IRQ output signal
55	NC	-	-	-
56	VCC	VCC	power	Digital IO power
57	VMICEXT	VMICEXT	AO	External MIC bias

58	MICIN	MICINL MIC0LN	AI	MICL channel input MIC0L Negative channel input when use as differential
59	VRO	VRO	AO	VR output
60	VREFI	VREFI	AIO	Reference Voltage, with capacitance
61	VROS	VROS	AO	VRO SENSE
62	FMINR	FMINR	AI	FMR channel input
63	FMINL	FMINL MICINLP	AI	FML channel input MIC0L Positive channel input when use as differential
64	OUTFL	OUTFL	AO	Front left channel output
65	OUTFR	OUTFR	AO	Front right channel output
66	NC	-	-	-
67	SGPIO5	SGPIO5	DIO	General Purpose Input/Output 5 SVCC
		IR LOSC_32K PWM1	AIO	IR control input 32K clock output PWM output1
68	SGPIO4	SGPIO4	DIO	General Purpose Input/Output 4 SVCC
		IR LOSC_32K	AIO	IR control input 32K clock output
69	EPAD	-	-	Ground

14 Package and Ordering Information

14.1 Package Drawing



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	5.40	5.50	5.60
E2	5.40	5.50	5.60
e	0.30	0.40	0.50
H	0.35REF		
K	0.70	–	–
L	0.30	0.40	0.50
R	0.09	–	–

Figure 14-1 ATC2603C Package Drawing

Appendix

Acronyms and Terms

AMIC	Analog Microphone
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
BT	Bluetooth
CC	Constant Current
CV	Constant Voltage
DC-DC/DC-DC	DC to DC Converter
DAC	Digital-to-Analog Converter
GPIO	General Purpose Input/Output
HW	Hardware
IR	Infrared
I/O	Input/Output
I2S	Inter-IC Sound
LSB	Least Significant Bit
Li-Ion	Lithium Ion (battery type)
LDO	Low Dropout Regulator
MIC	Microphone
MSB	Most Significant Bit
OS	Operation System
OSC	Oscillator
PA	Power Amplifier
PMIC	Power Management Integrated Circuit
PMU	Power Management Unit
PDM	Pulse Distance Modulation
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
RTC	Real-Time Clock
SCY	Sampling Cycle
SD	Secure Digital memory card
SW	Software
SoC	System on Chip
THD	Total Harmonic Distortion
UART	Universal Asynchronous Receiver Transmitter

Actions (Zhuhai) Technology Co., Limited
Address: No. 1 / C, Ke Ji Si Road, Hi-Tech Zone, Tangjia, Zhuhai
Tel: +86-756-3392353
Fax: +86-756-3392251
Post Code: 519085
http://www.actions-semi.com
Business Email: mp-sales@actions-semi.com
Technical Service Email: mp-cs@actions-semi.com